

Compal Confidential

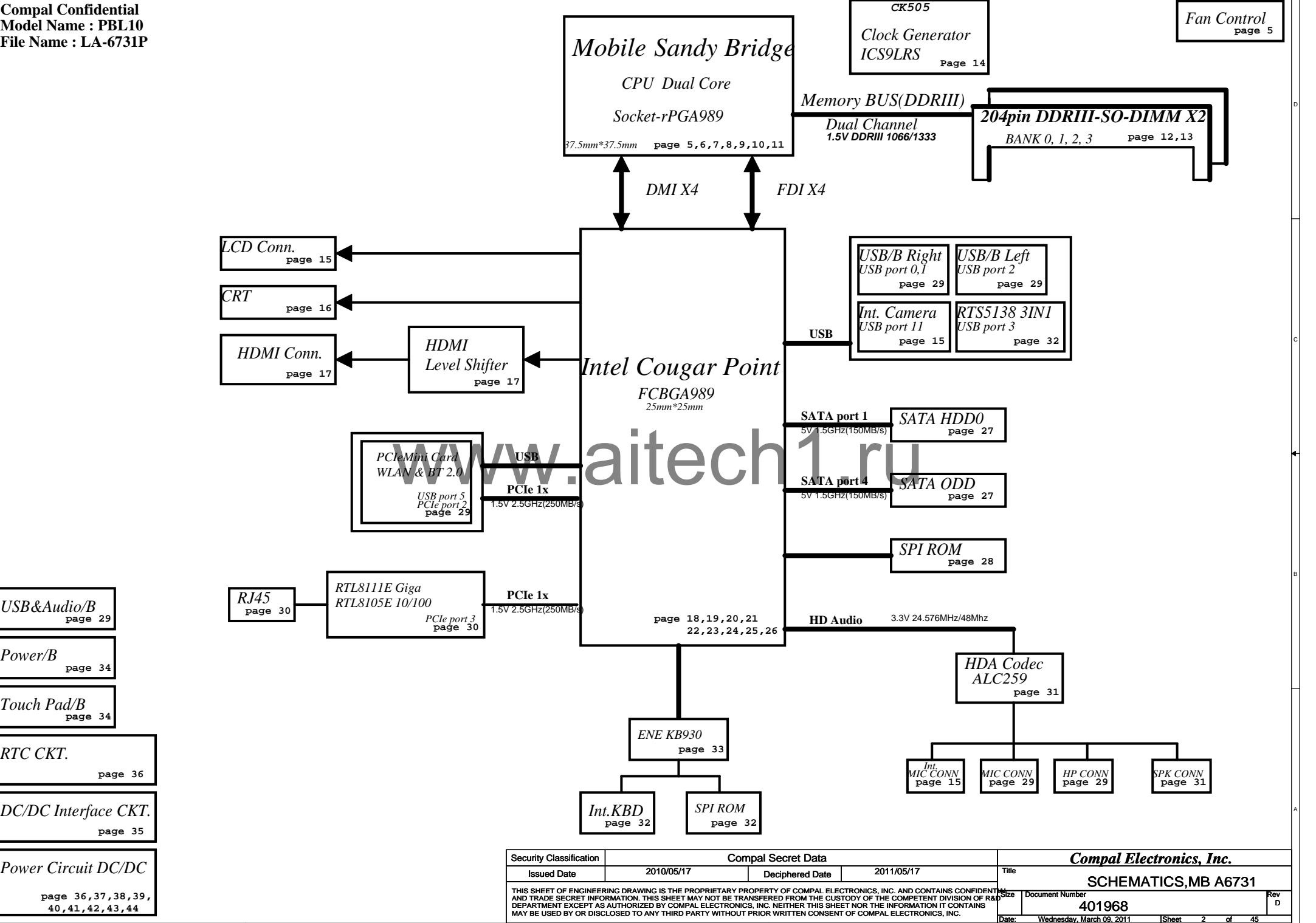
PBL10 Project

LA-6731P REV1.0 Schematic

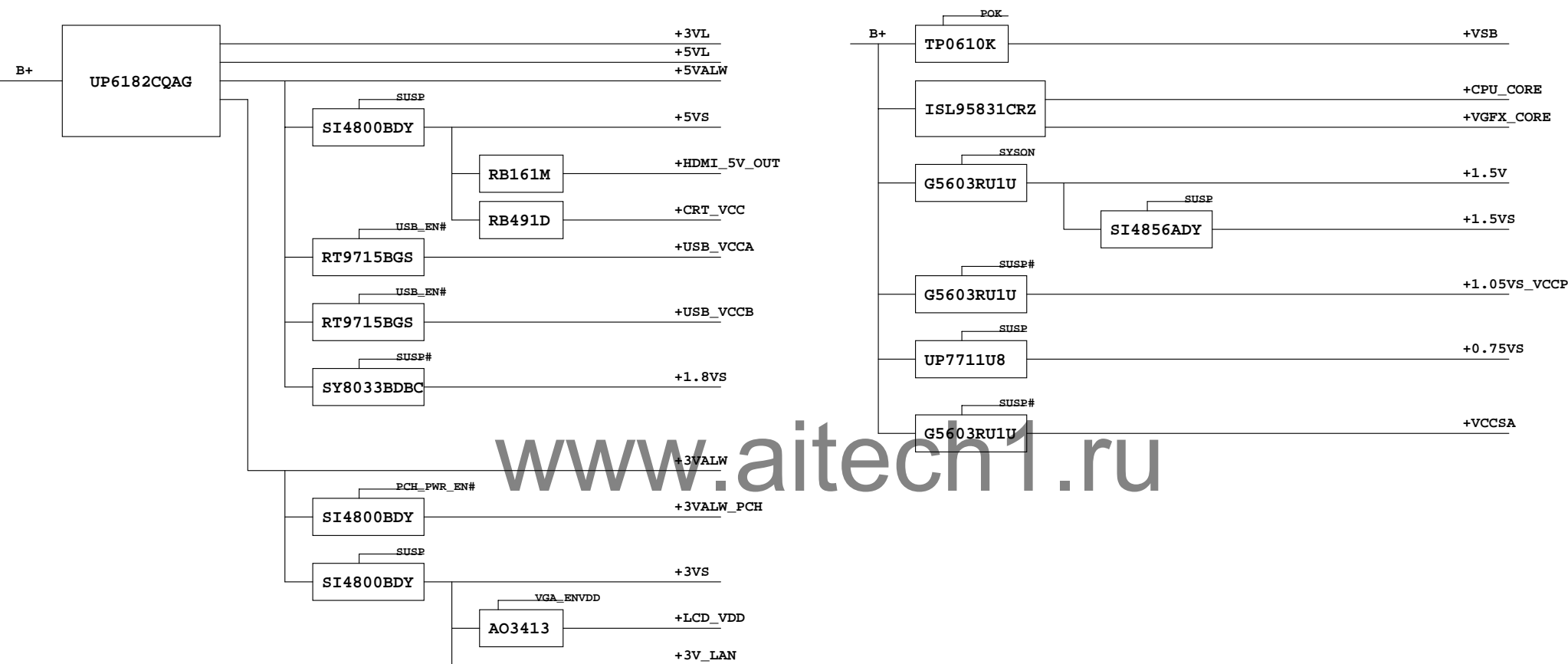
Intel Sandy Bridge/Cougar Point(UMA)

2010-12-06 Rev 1.0

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Issued Date	2010/05/17	Deciphered Date	2011/05/17	Title	SCHEMATICS,MB A6731	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address






Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM configu table

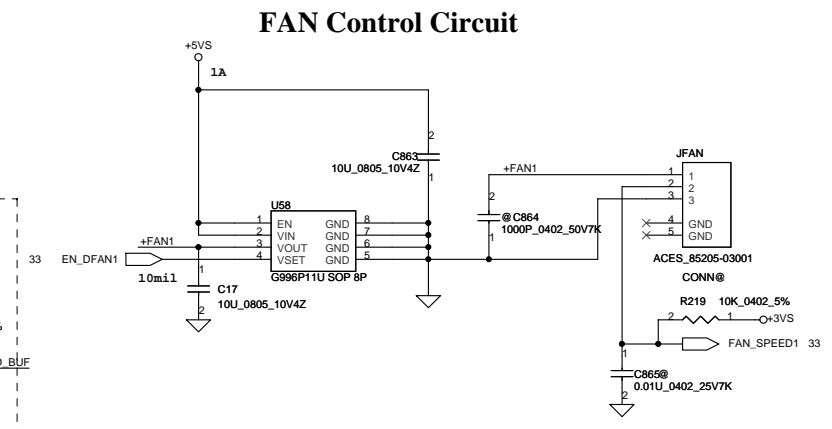
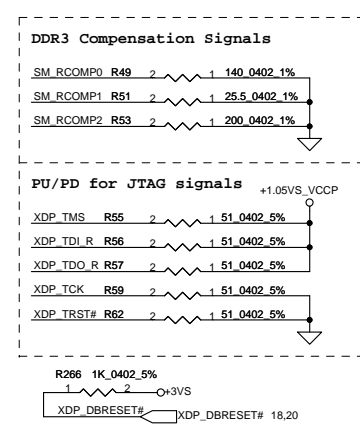
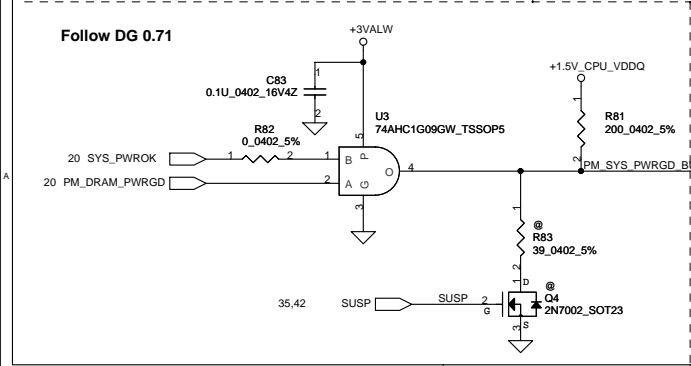
	SKU	Bom config	Description
1	46196830L01	DA6@/HDMI@/8105E@/PCH@	PBL10 UMA DUAL 10-100
2	46196830L02	DA6@/HDMI@/8111E@/PCH@	PBL10 UMA DUAL GIGA LAN
3			
4			
5			
6			
7			
8			

Bom configu(HDMI@/8105E@/8111E@/DA6@/DAZ@/45@)

PCH And PCBA table

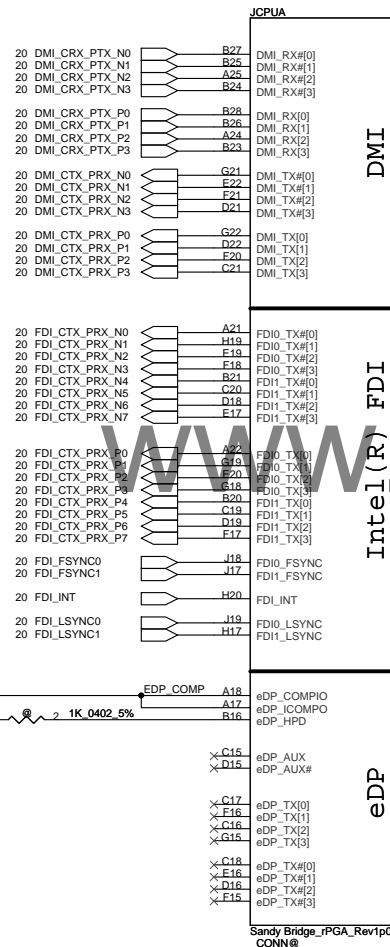
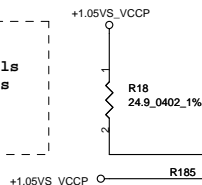
PCH	 U4 BD82HM65 SLH9D B2 FCBGA 989P PCH PCH@			
PCB	 ZZZ DAZ@ PCB LA-6731P REV10	 ZZZ DA6@ PCB LA-6731P REV10	 ZZZ DA4@ PCB LS-6732P REV10	 ZZZ DA2@ PCB LS-6731P REV10

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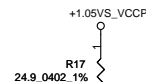


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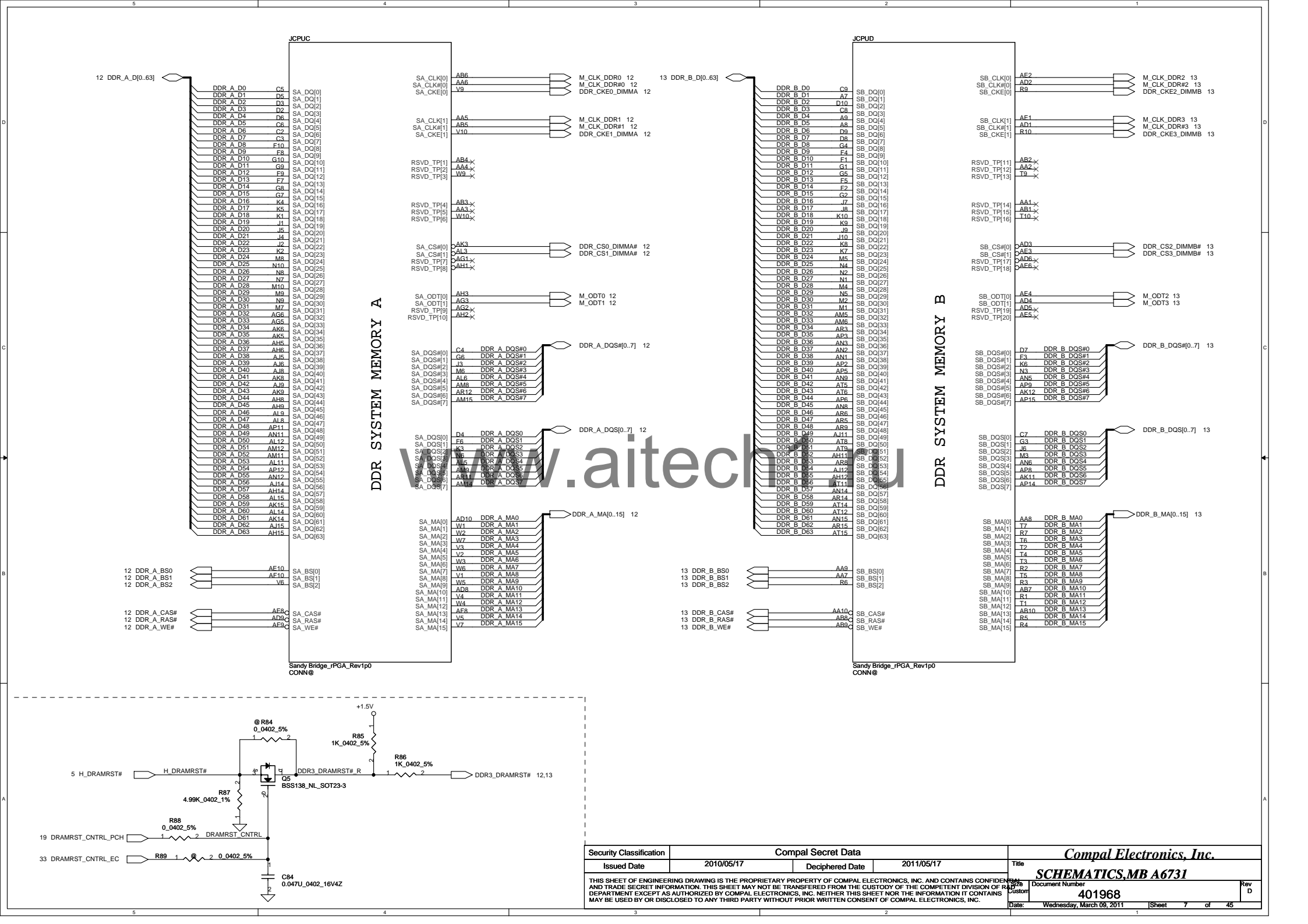
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



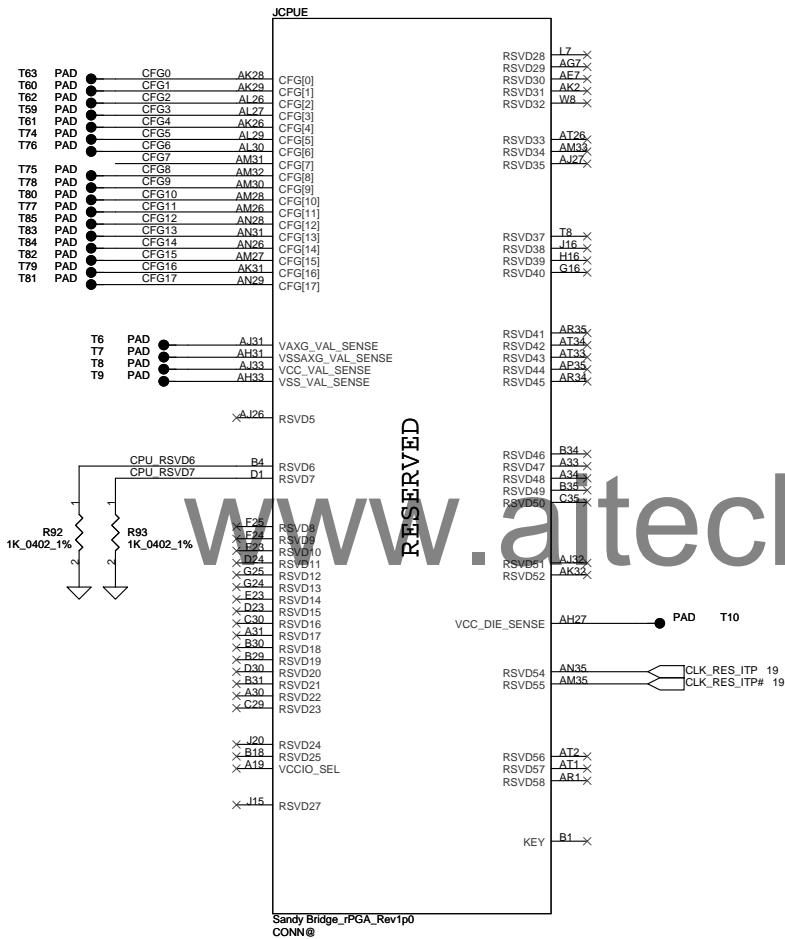
PCI EXPRESS * - GRAPHICS



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

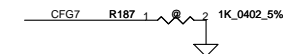


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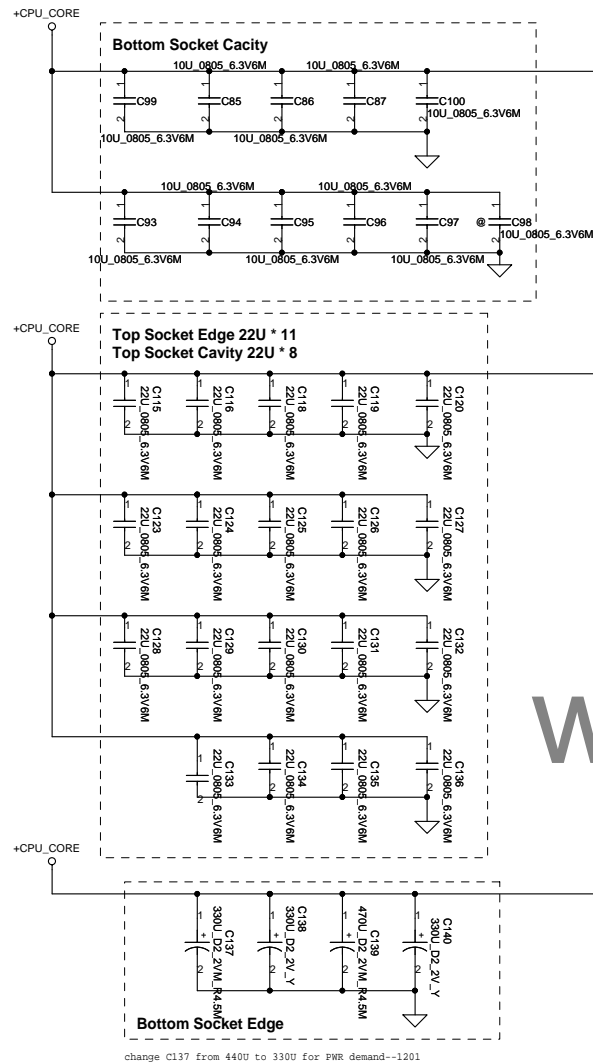


CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



POWER



change C137 from 440U to 330U for PWR demand--1201

94A

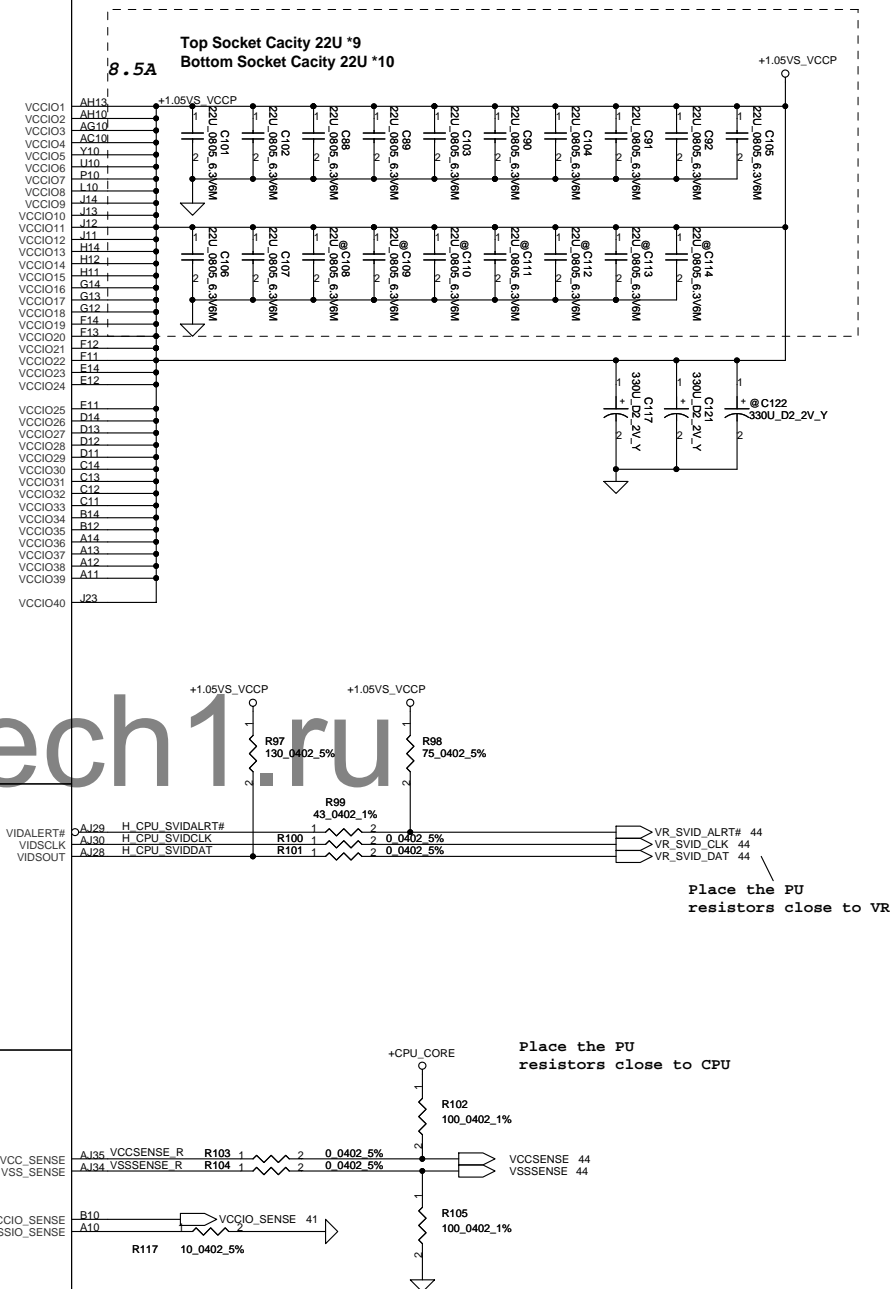
AG35	VC01
AG34	VC02
AG33	VC03
AG32	VC04
AG31	VC05
AG30	VC06
AG29	VC07
AG28	VC08
AG27	VC09
AG26	VC10
AG25	VC11
AF34	VC12
AF33	VC13
AF32	VC14
AF31	VC15
AF29	VC16
AF28	VC17
AF27	VC18
AD35	VC19
AD34	VC20
AD33	VC21
AD32	VC22
AD31	VC23
AD30	VC24
AD29	VC25
AD28	VC26
AD27	VC27
AD26	VC28
AC35	VC29
AC34	VC30
AC33	VC31
AC32	VC32
AC31	VC33
AC29	VC34
AC28	VC35
AC27	VC36
AC26	VC37
AA35	VC38
AA34	VC39
AA33	VC40
AA32	VC41
AA31	VC42
AA30	VC43
AA29	VC44
AA28	VC45
AA27	VC46
AA26	VC47
Y35	VC48
Y34	VC49
Y33	VC50
Y32	VC51
Y31	VC52
Y30	VC53
Y29	VC54
Y28	VC55
Y27	VC56
Y26	VC57
Y25	VC58
Y24	VC59
Y23	VC60
Y22	VC61
Y21	VC62
Y20	VC63
Y19	VC64
Y18	VC65
Y17	VC66
Y16	VC67
Y15	VC68
Y14	VC69
Y13	VC70
Y12	VC71
Y11	VC72
Y10	VC73
Y09	VC74
Y08	VC75
Y07	VC76
Y06	VC77
Y05	VC78
Y04	VC79
Y03	VC80
Y02	VC81
R35	VC82
R34	VC83
R33	VC84
R32	VC85
R31	VC86
R30	VC87
R29	VC88
R28	VC89
R27	VC90
R26	VC91
R25	VC92
P35	VC93
P34	VC94
P33	VC95
P32	VC96
P31	VC97
P30	VC98
P29	VC99
P28	VC100
P27	
P26	

CORE SUPPLY

SVID

SENSE LINES

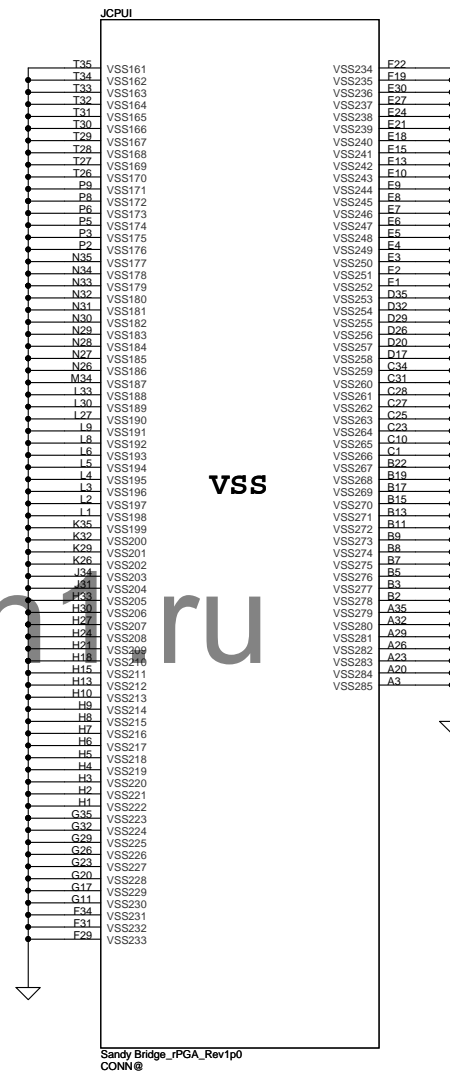
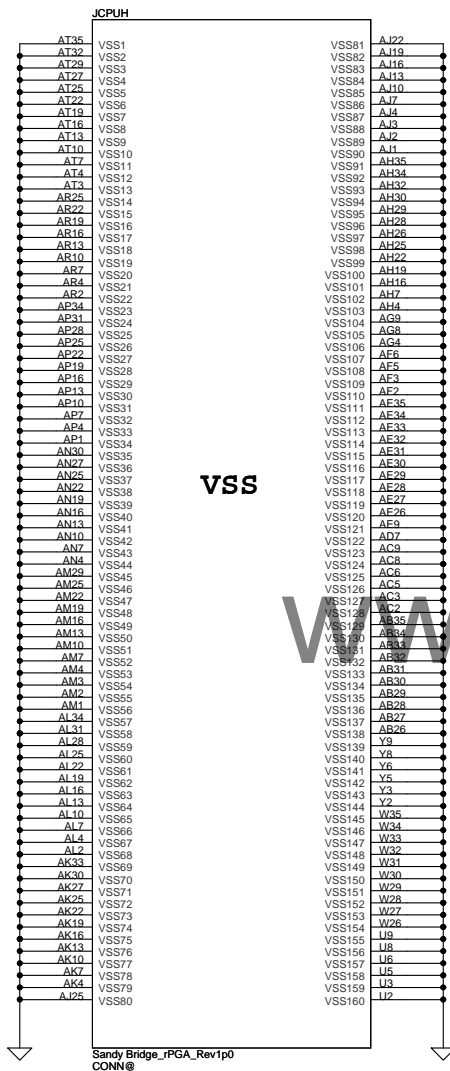
PEG AND DDR

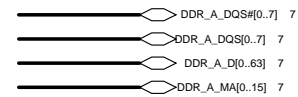
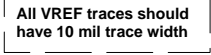


Sandy Bridge_rPGA_Rev1p0
CONN@

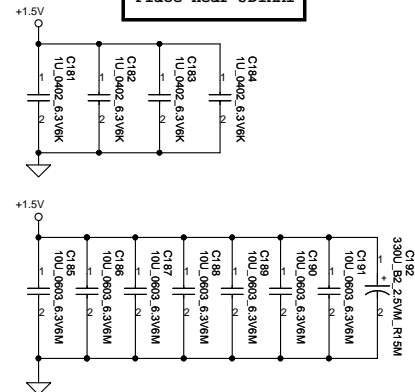
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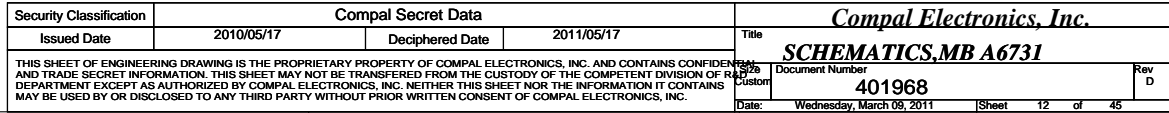
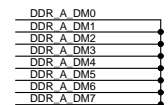
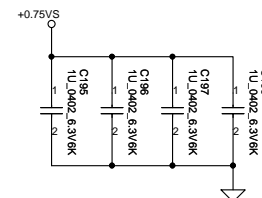




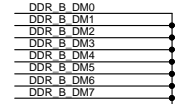
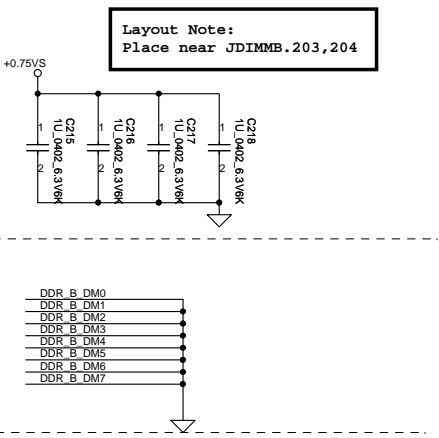
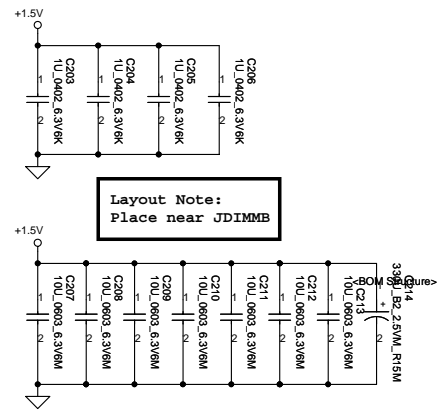
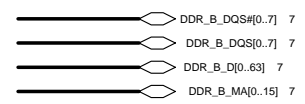
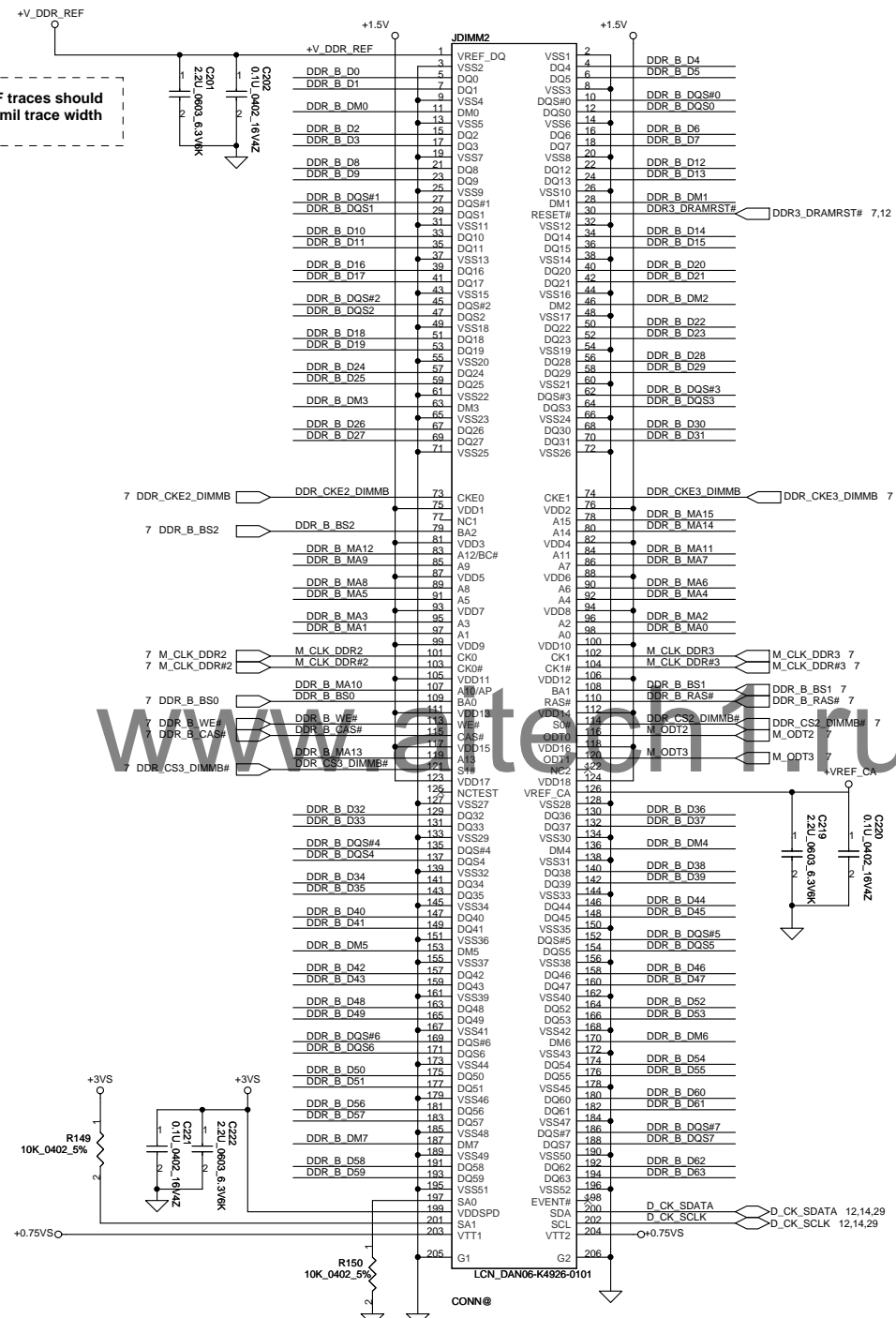
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204

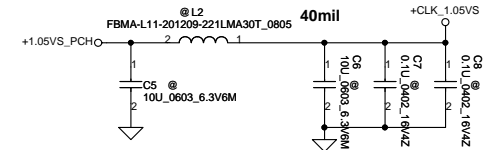
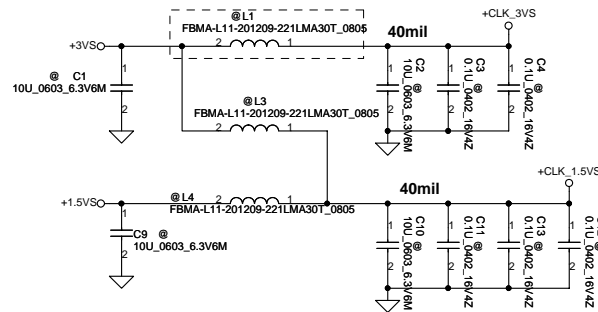


All VREF traces should have 10 mil trace width



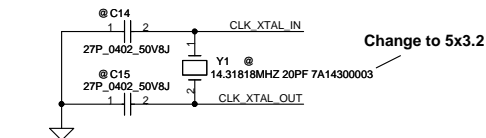
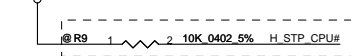
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SM010014520 3000ma 220ohm@100mhz DCR 0.04

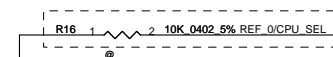


Use internal Clock first, reseve external clock.

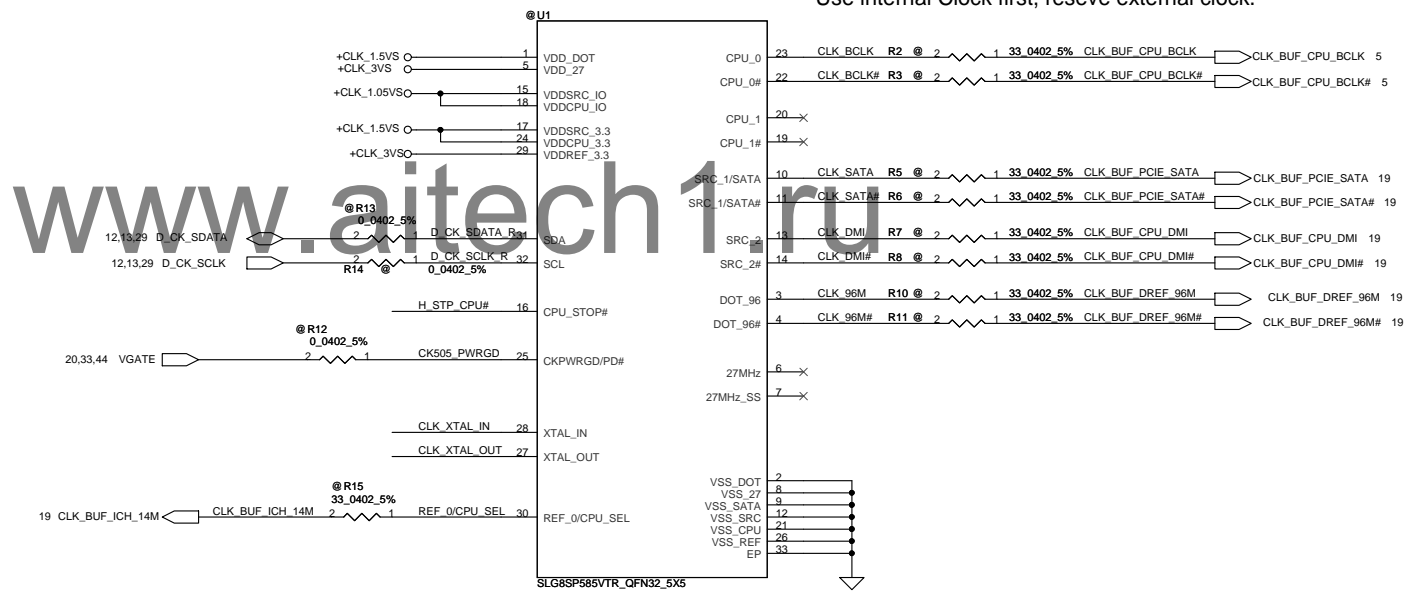
Silego Have Internal Pull-Up
IDT 9LVS3199AKLFT NC



IDT Have Internal Pull-Down
FOR Realtek

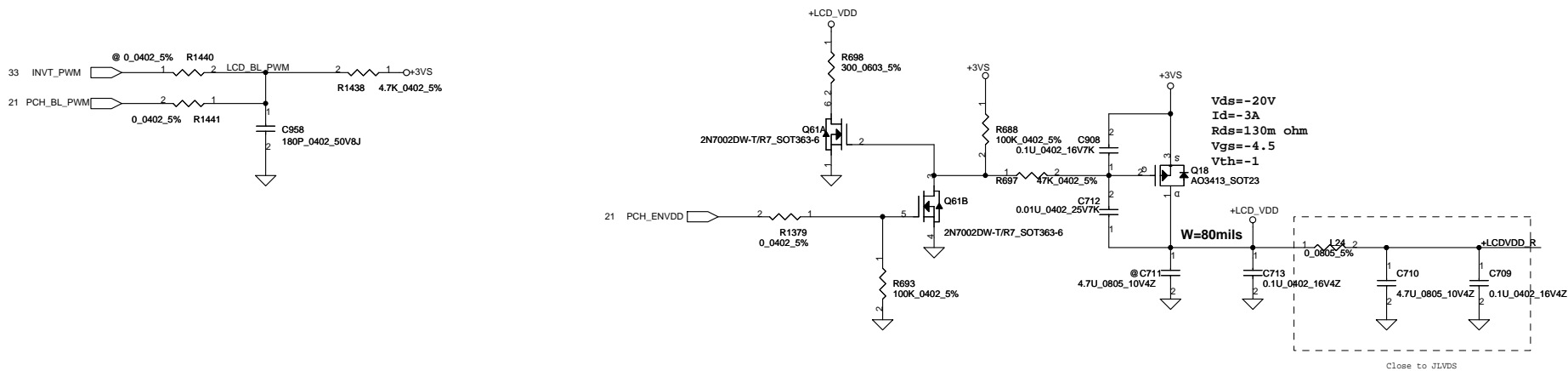


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

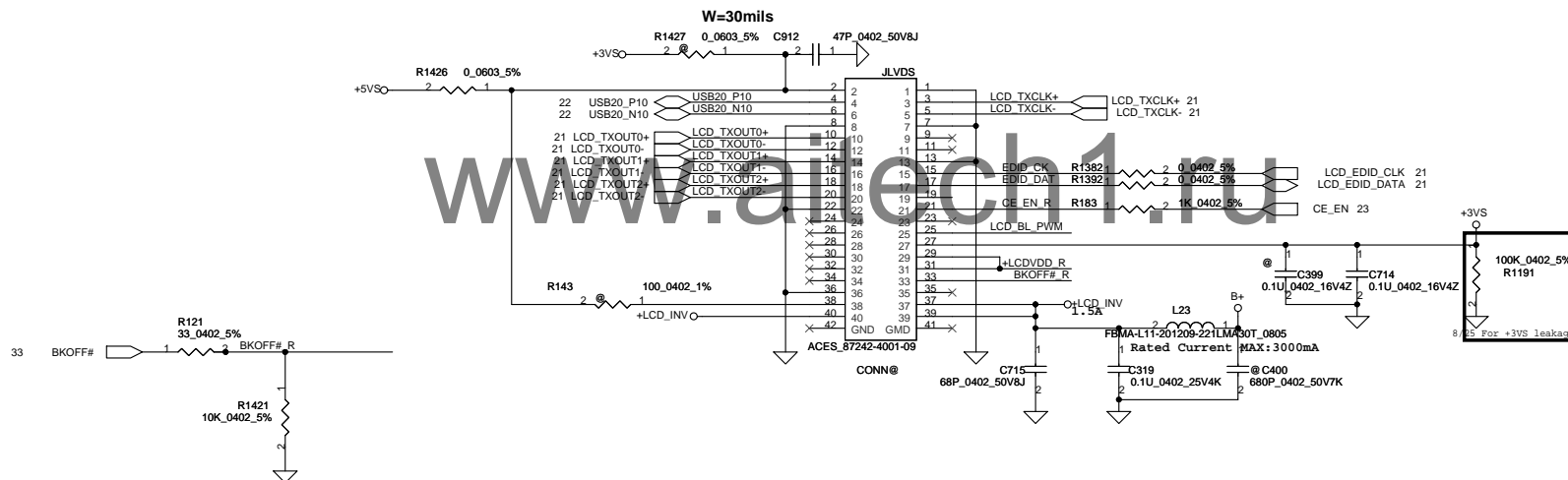


Standard
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10

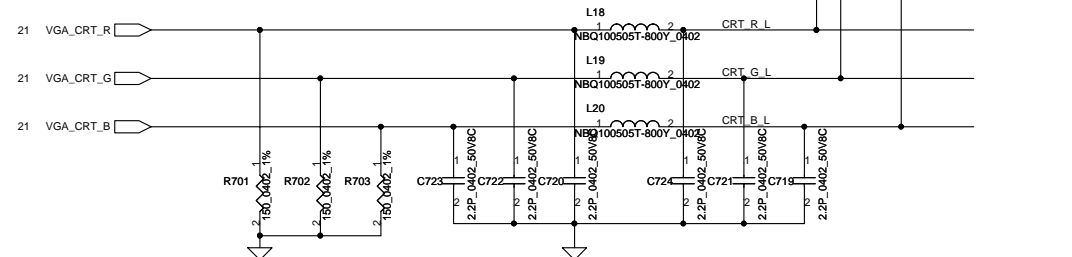
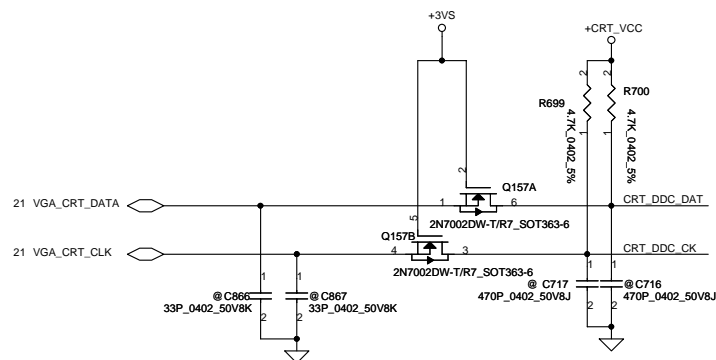
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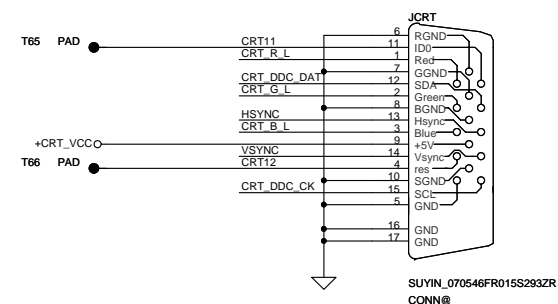
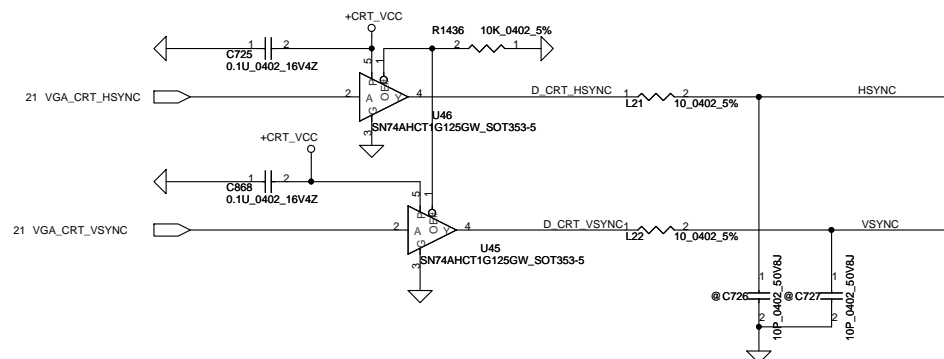
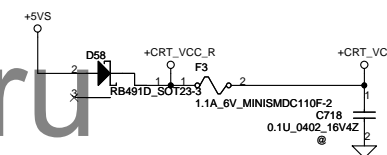
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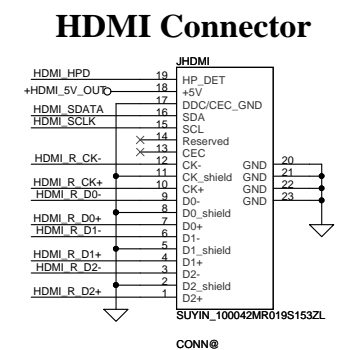
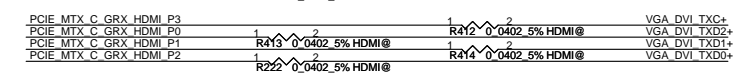
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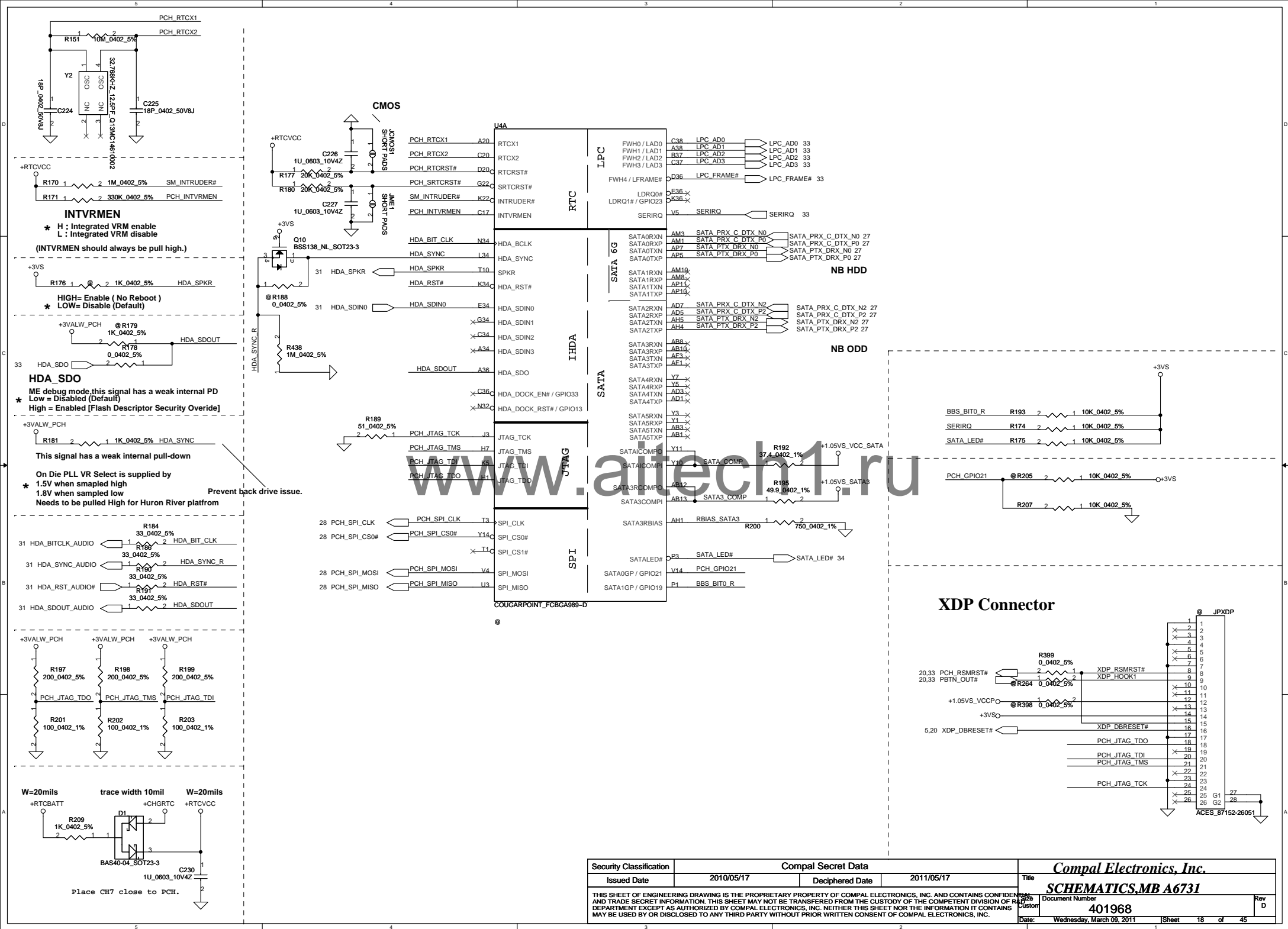
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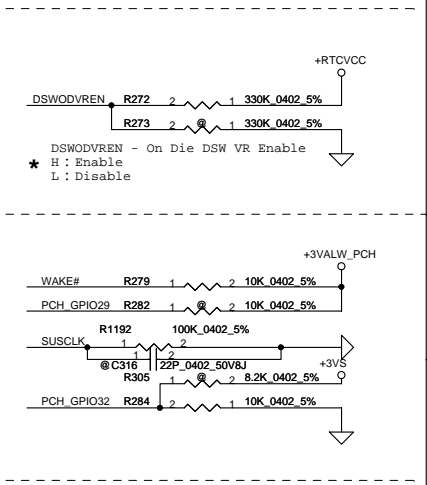
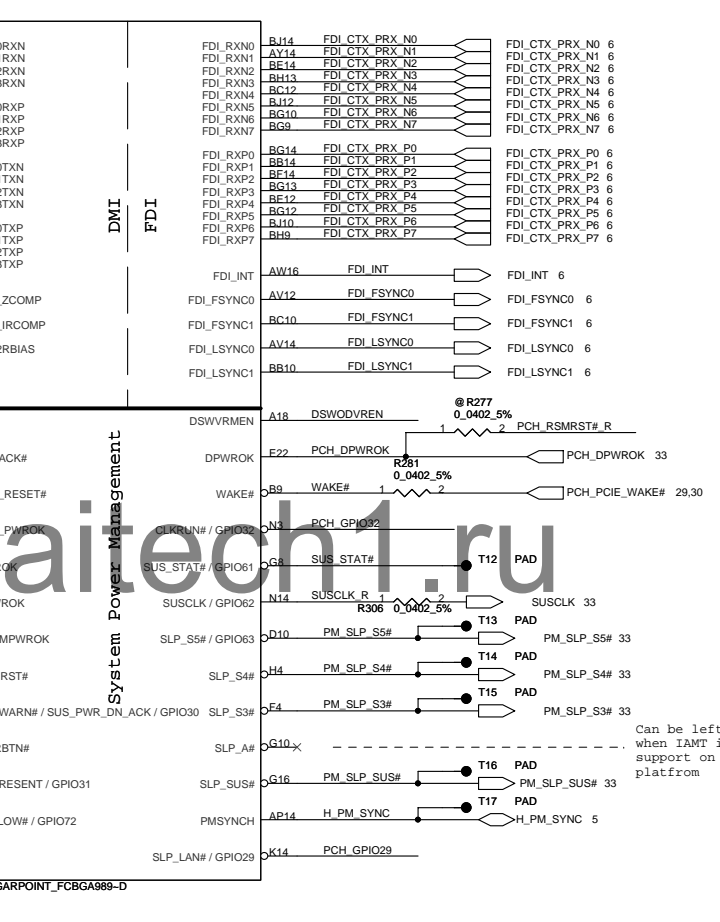
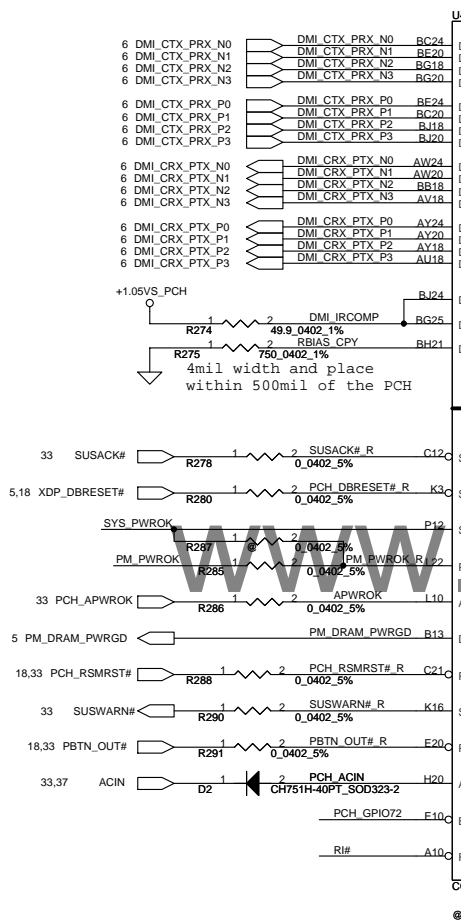
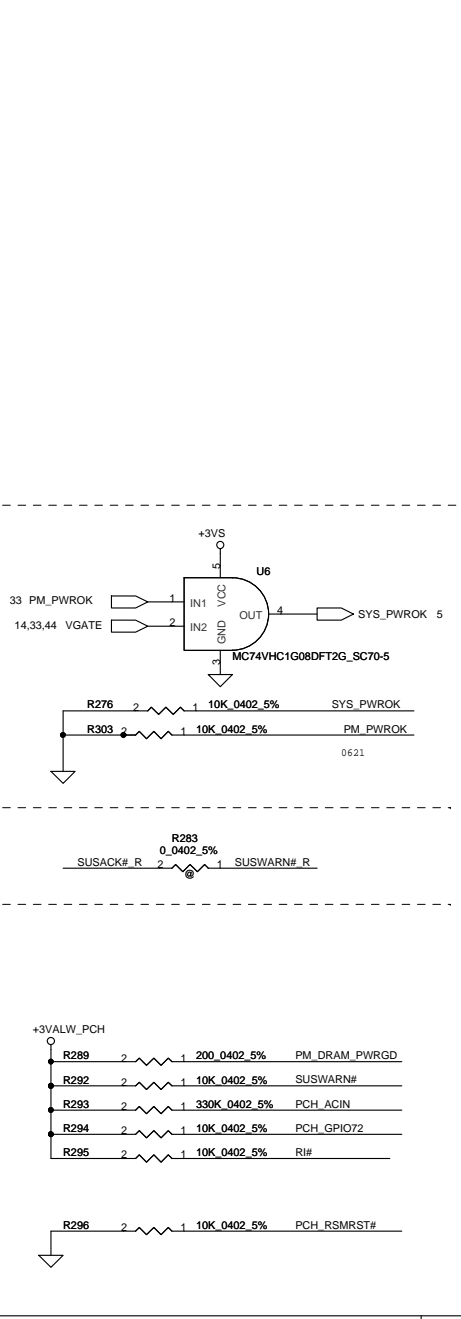


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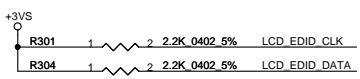
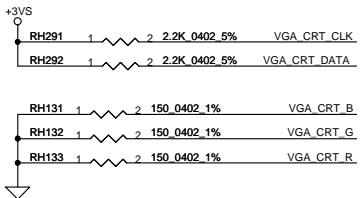
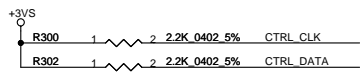
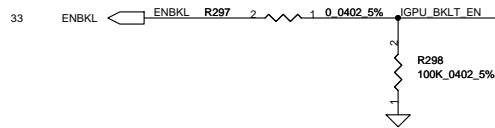


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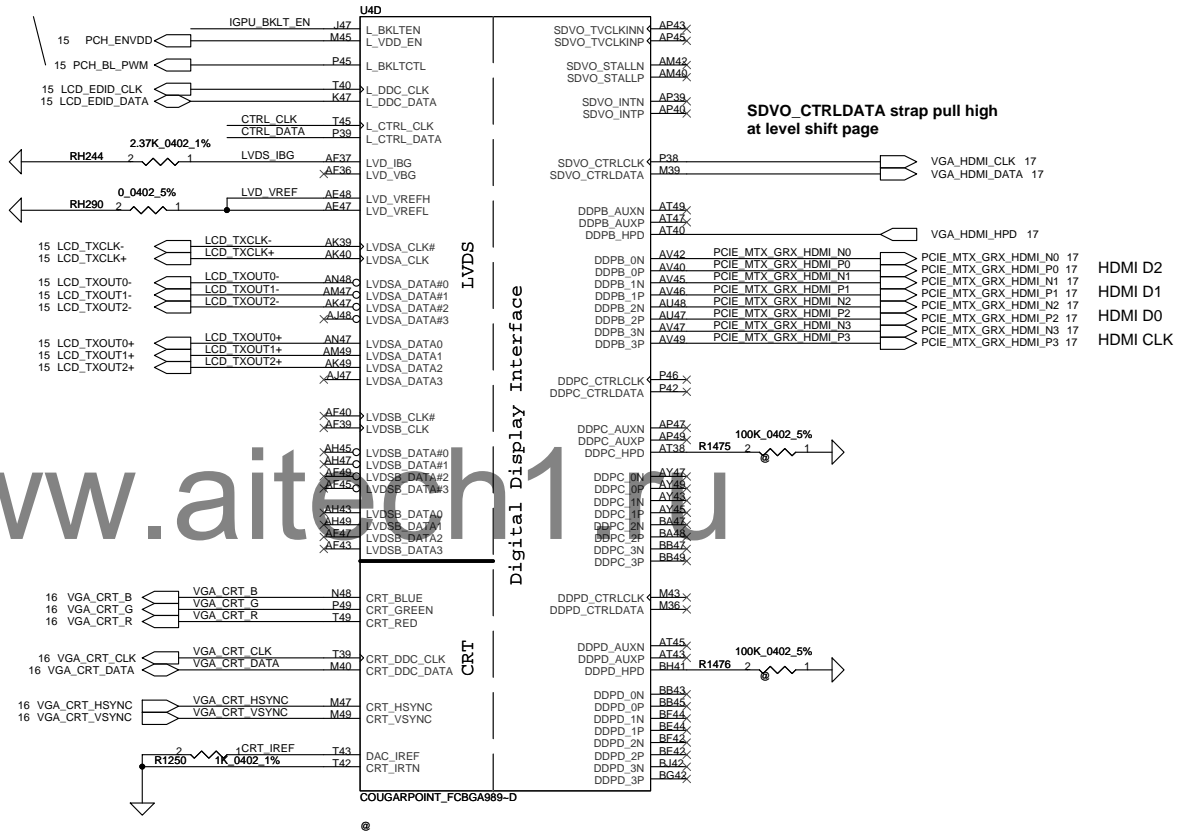




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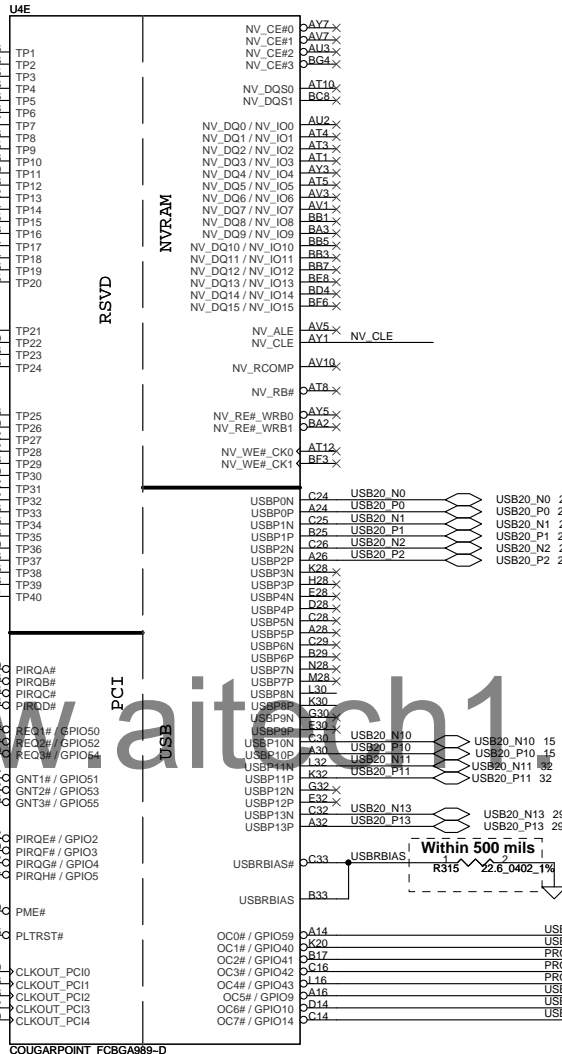
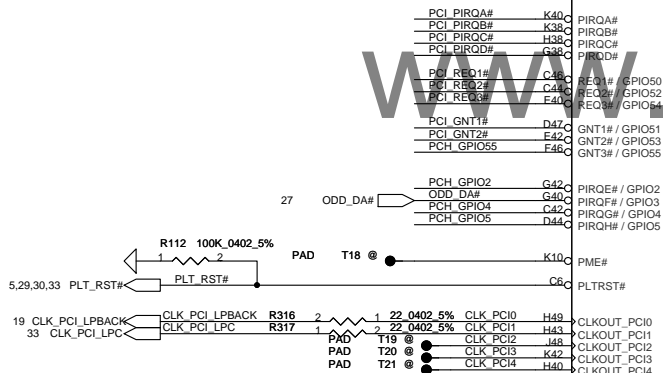
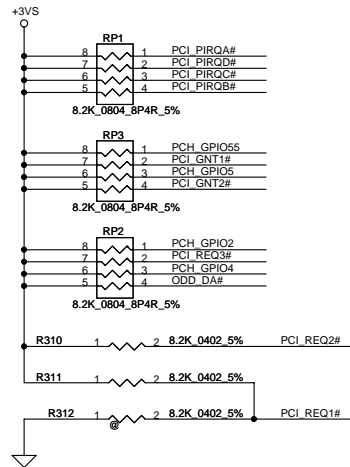


Pull high at LVDS conn side.

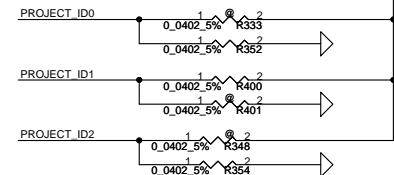
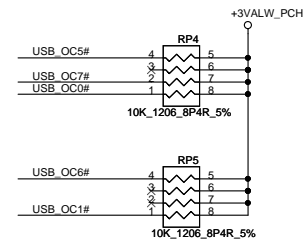
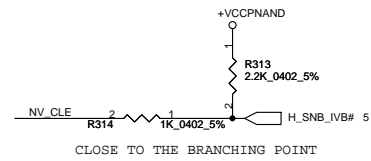


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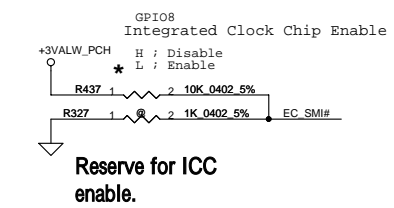


DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW



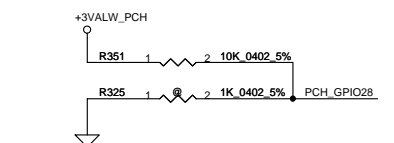
	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
PBL10	0	1	0
PBL11	0	1	1

Boot BIOS Strap bit1 BBS1			
BBS bit1 /BBS bit0	Bit11	Bit10	Boot BIOS Destination
0	1		Reserved
1	0		PCI
1	1		SPI *
0	0		LPC

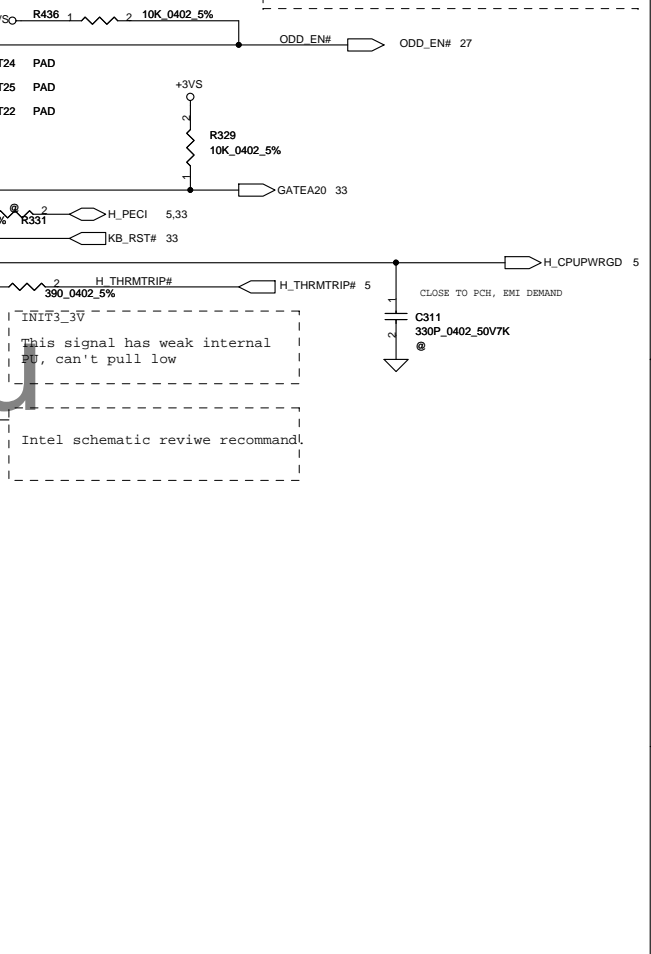
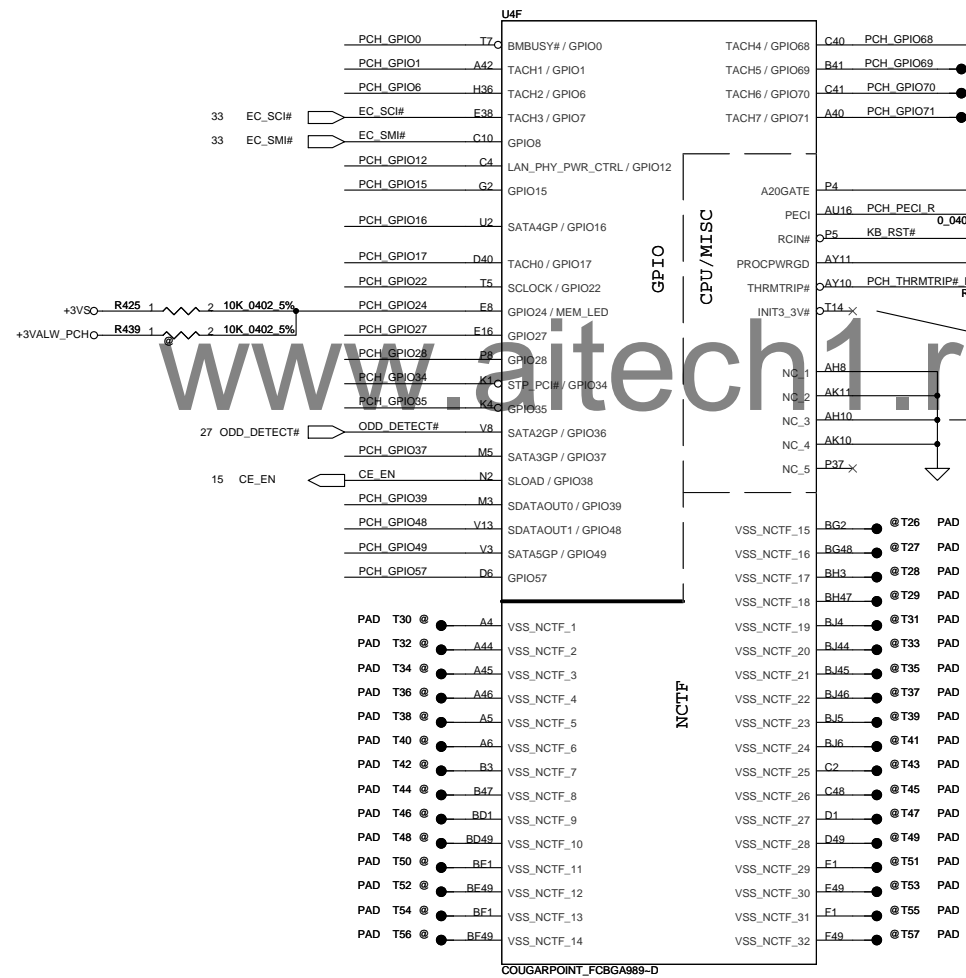
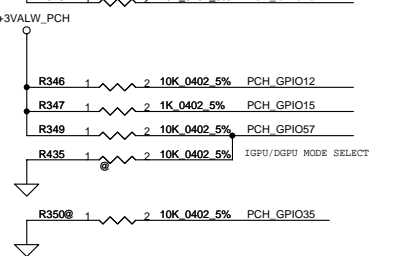
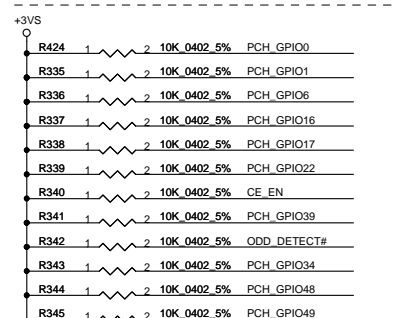
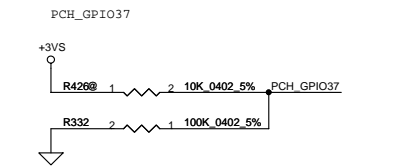
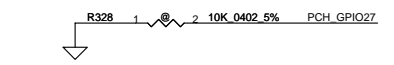


GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

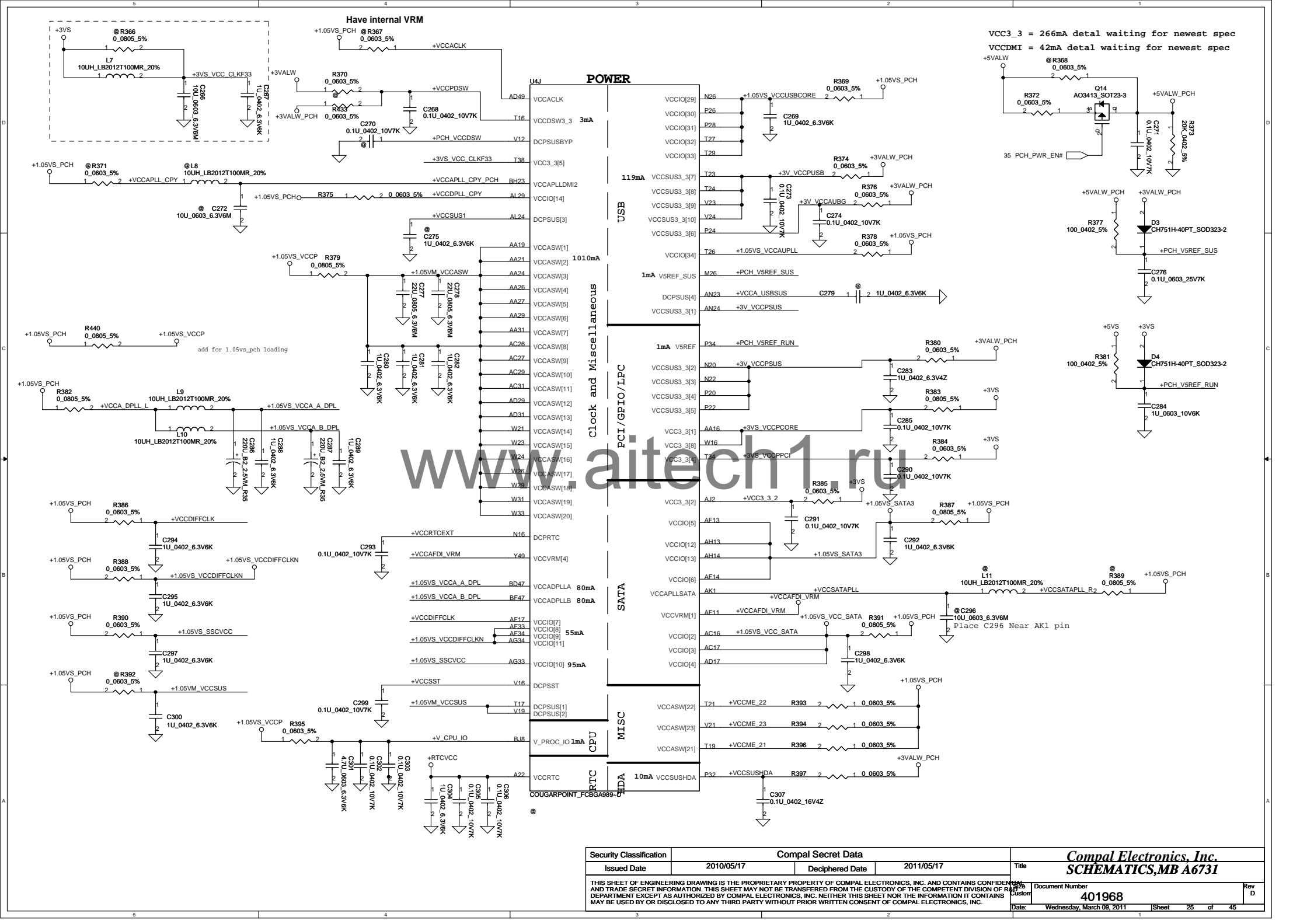
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



PCH_GPIO27 (Have internal Pull-High)
★High: VCCVRM VR Enable
Low: VCCVRM VR Disable



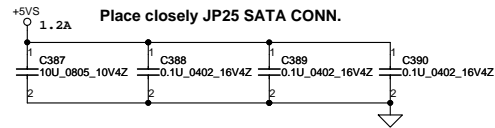
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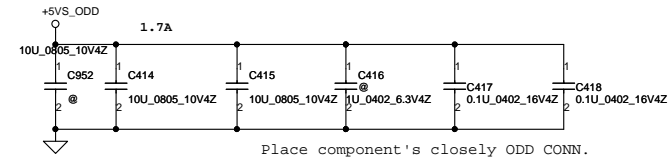


VSS[120]	AR48		R03	VSS[207]
VSS[121]	AT11		BF30	VSS[208]
VSS[122]	AT13		BF38	VSS[209]
VSS[123]	AT18		BF40	VSS[210]
VSS[124]	AT22		BF9	VSS[211]
VSS[125]	AT26		BG17	VSS[212]
VSS[126]	AT29		BG24	VSS[213]
VSS[127]	AT31		BG33	VSS[214]
VSS[128]	AT32		BG44	VSS[215]
VSS[129]	AT34		BG8	VSS[216]
	AT39		BH4	

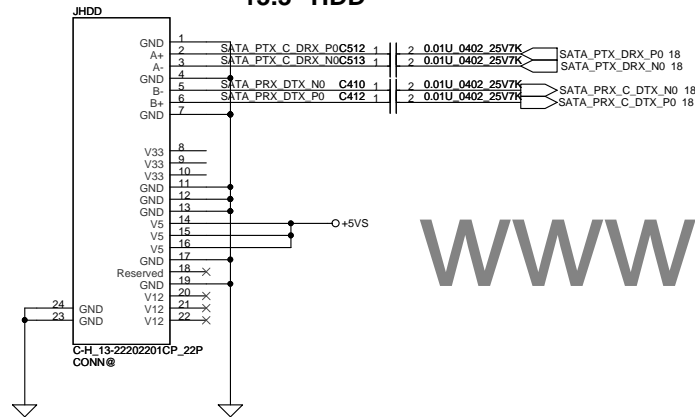
SATA HDD1 Conn.



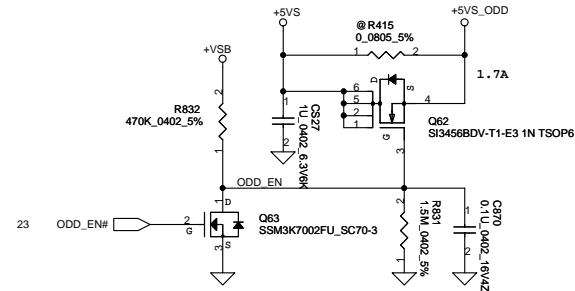
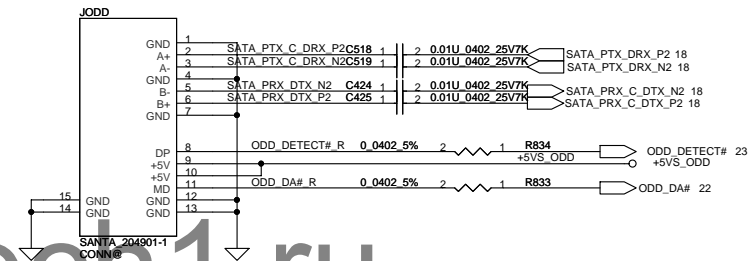
SATA ODD Conn



13.3" HDD

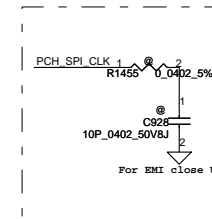
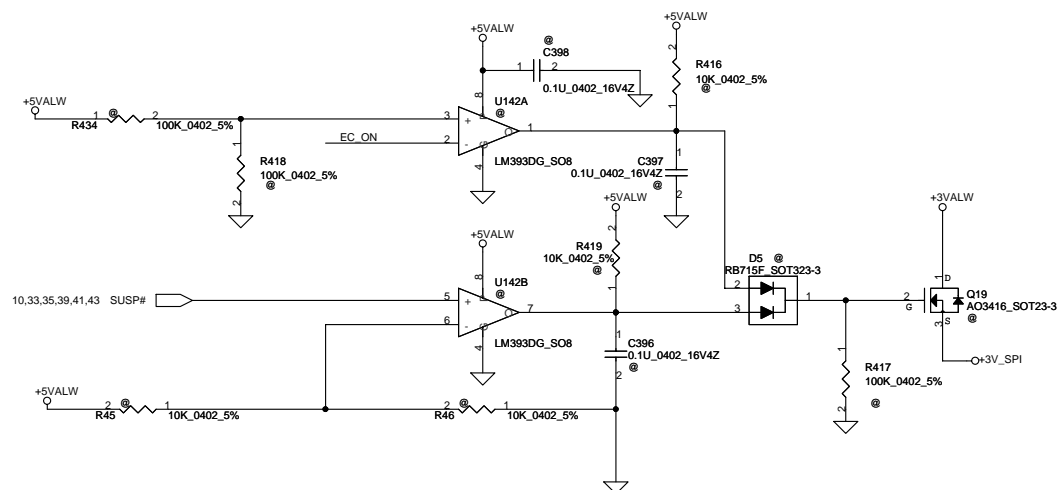


13.3" ODD

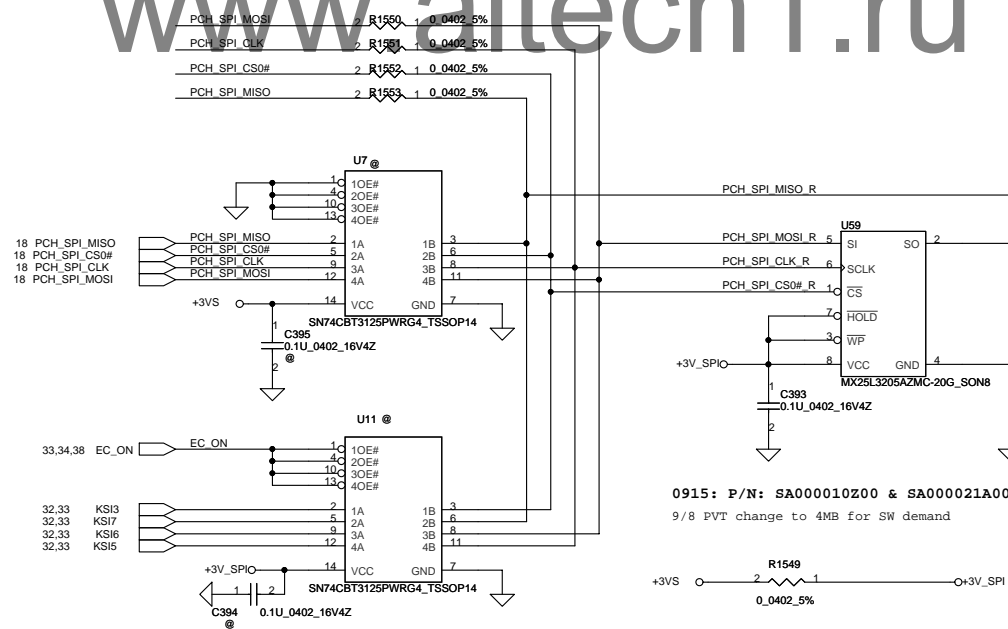


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**SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte**

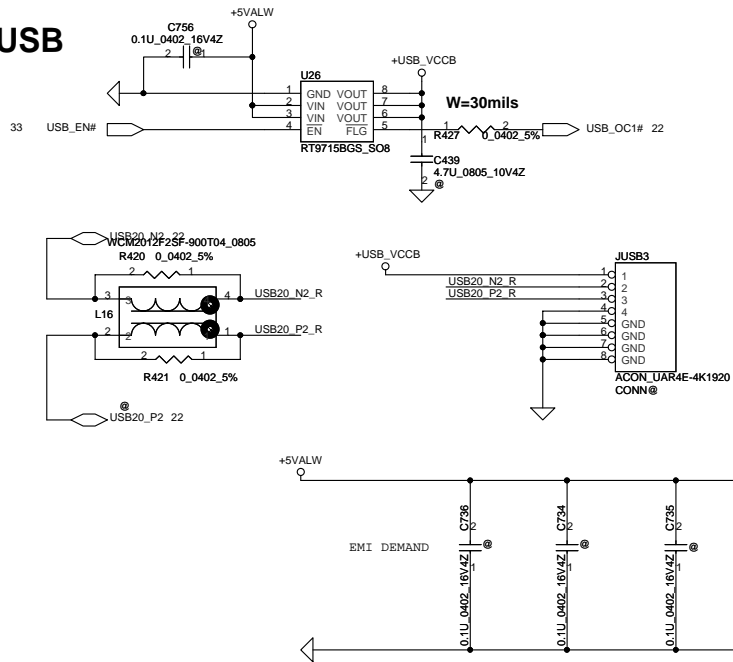


PCH SPI MOSI	R1550	0.0402	5%
PCH SPI CLK	R1551	0.0402	5%

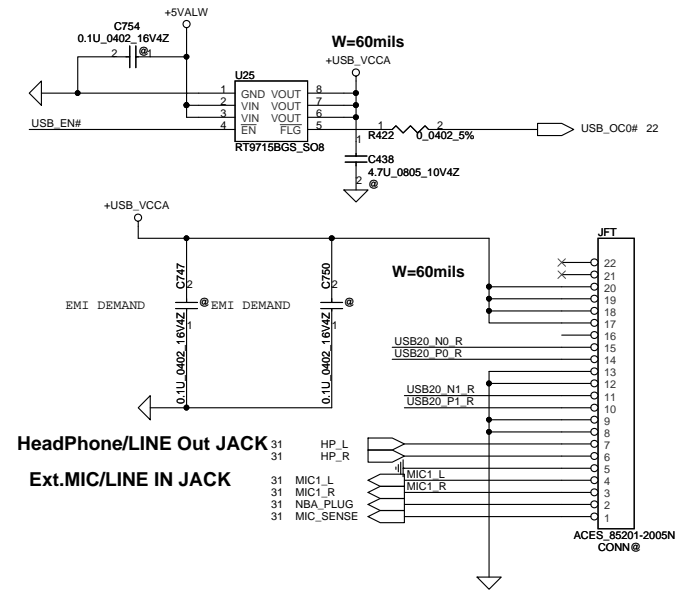
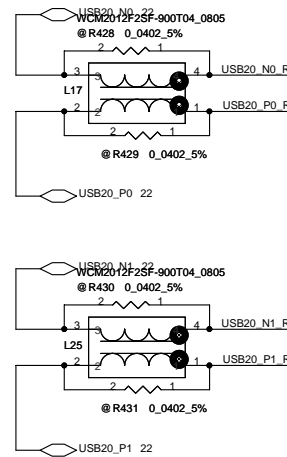


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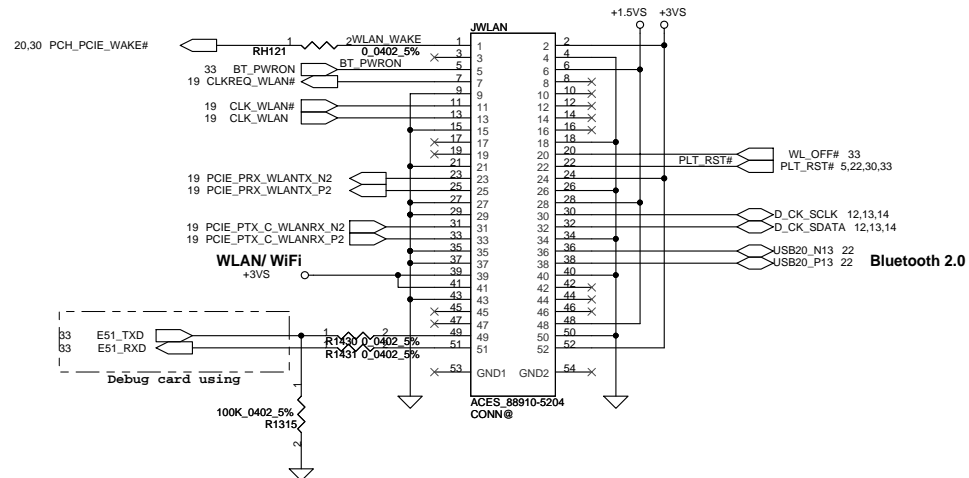
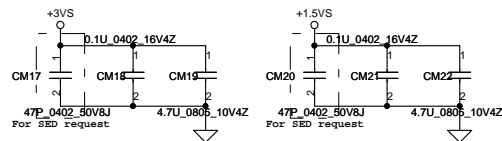
Left USB



Function Board



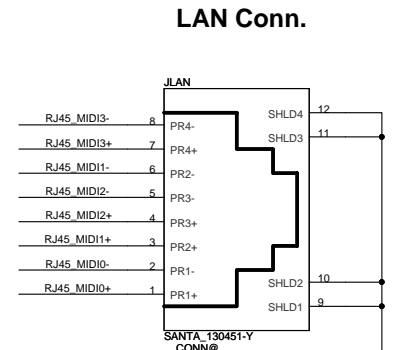
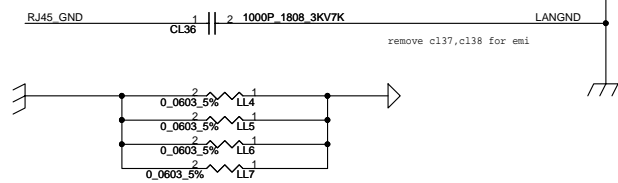
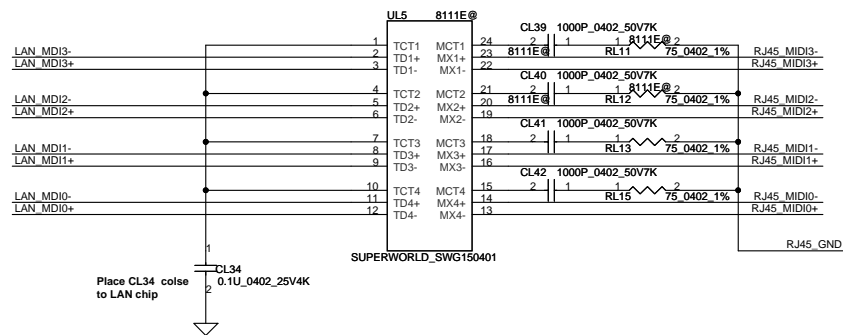
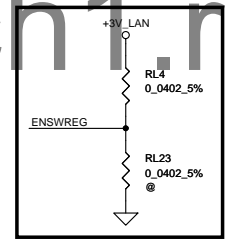
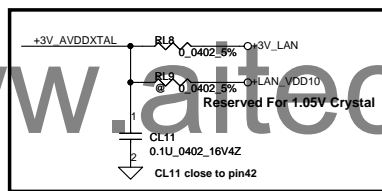
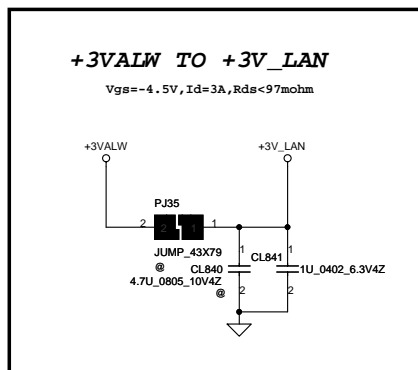
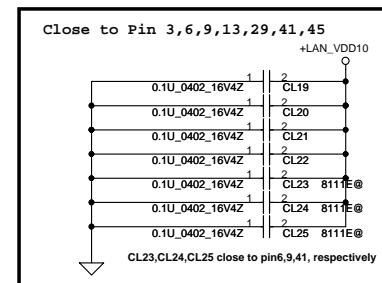
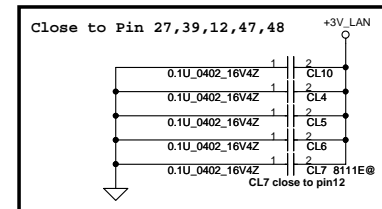
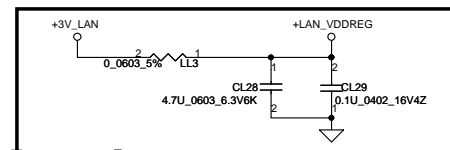
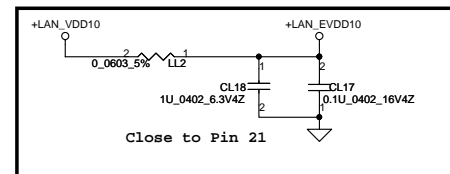
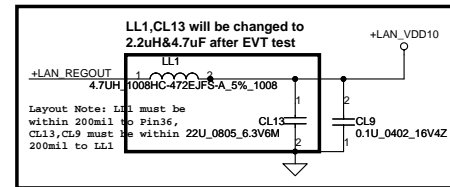
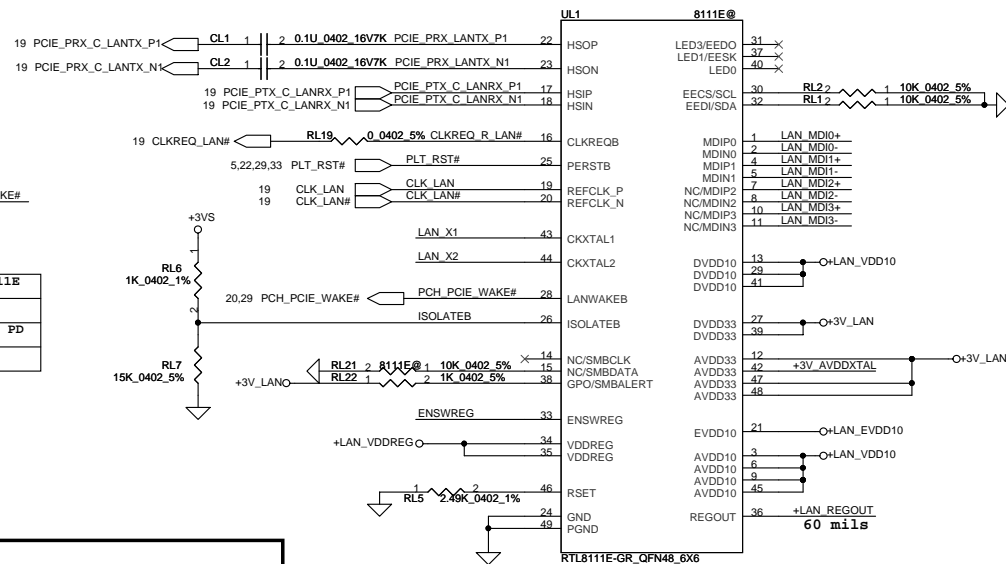
Slot 1 Half PCIe Mini Card-WLAN & BT2.0



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	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



For P/N and footprint
Please place them to ISPD page

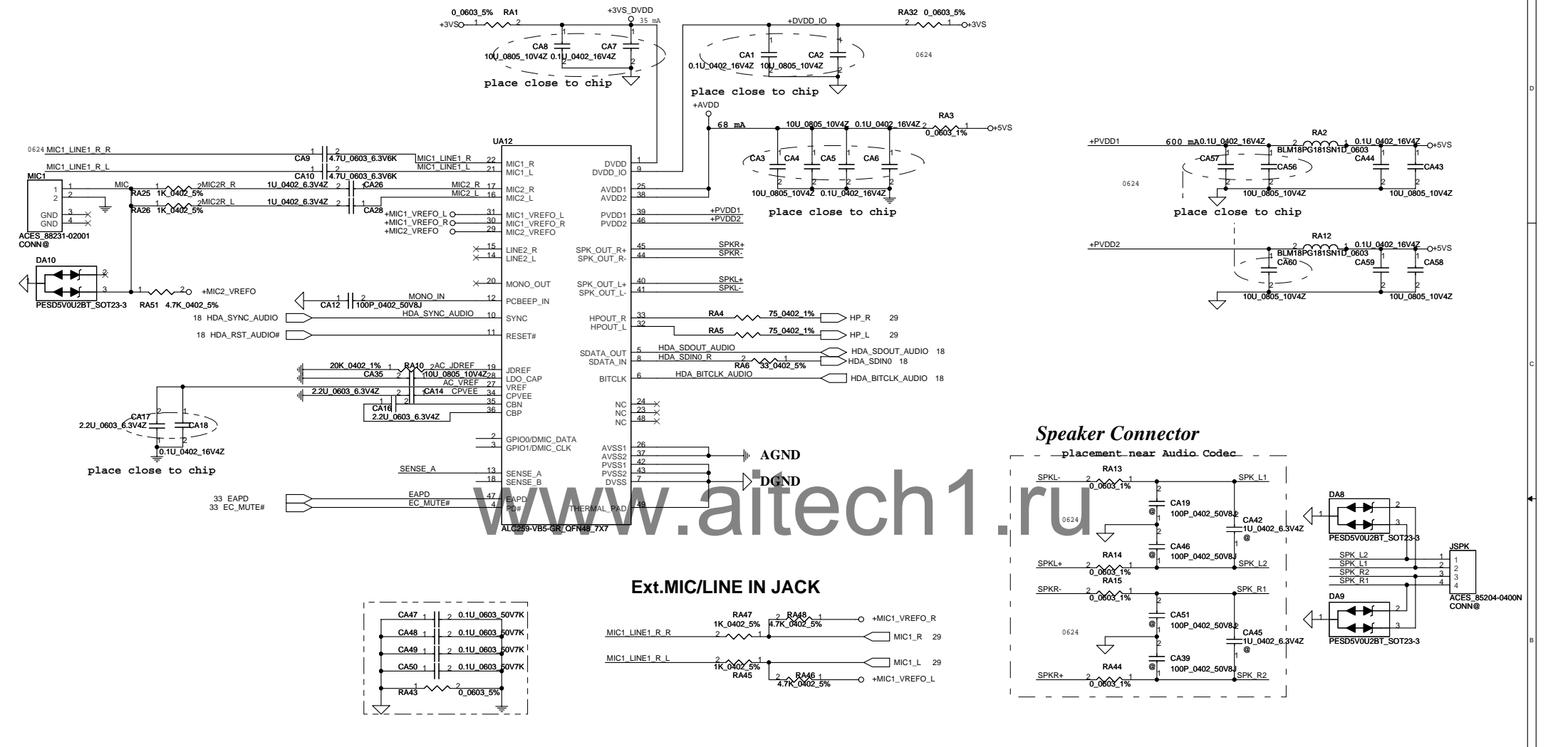
UL1

8105E 10/100M
8105E@

UL5

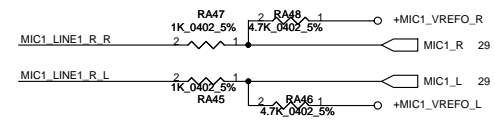
10/100M transformer
8105E@

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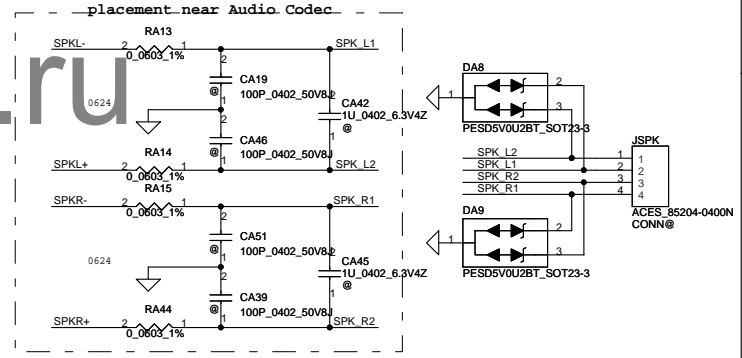


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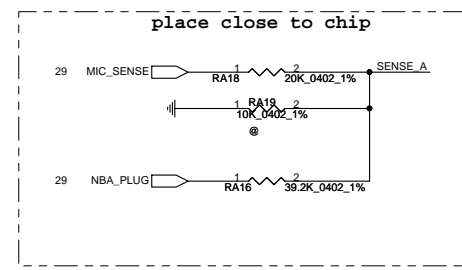
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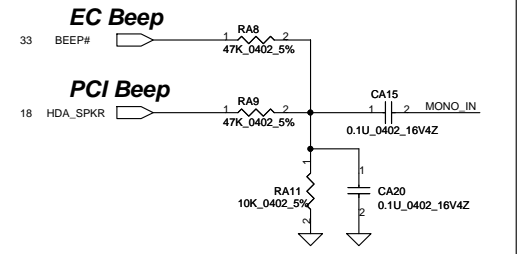
Speaker Connector



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

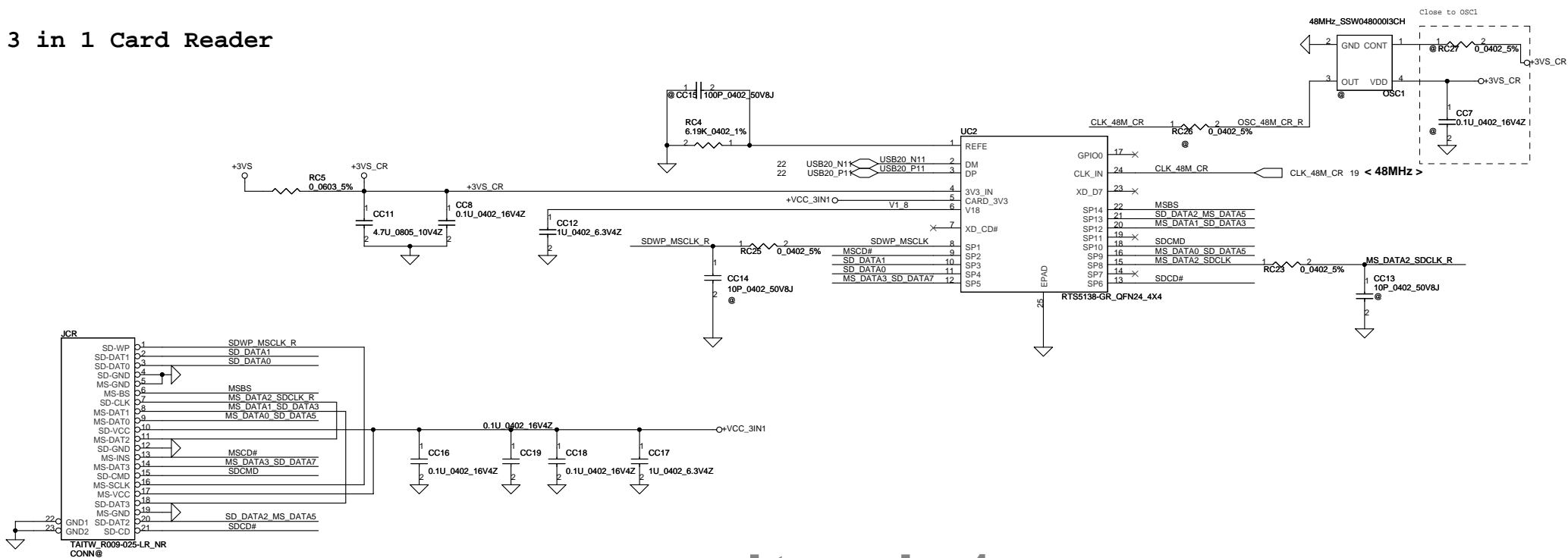


Beep sound



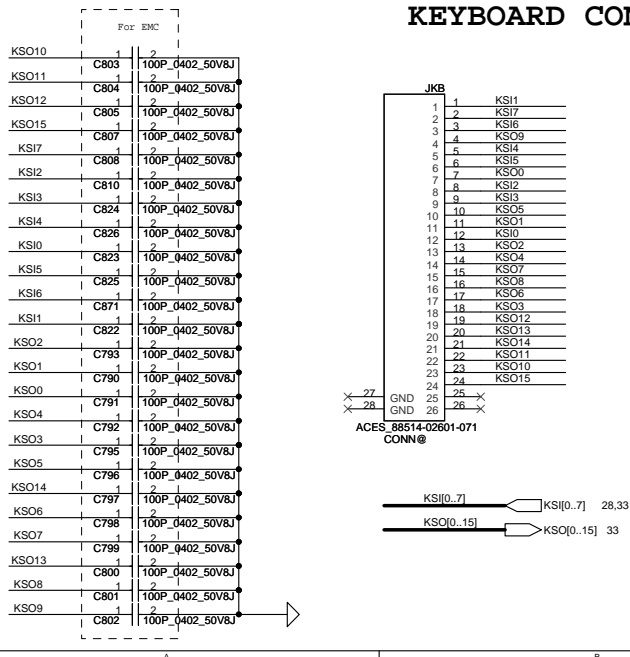
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3 in 1 Card Reader

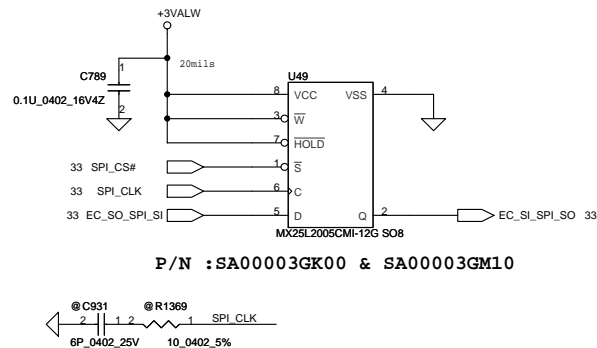


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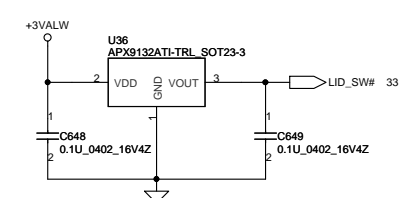
KEYBOARD CONN.



SPI Flash (1MByte*1)

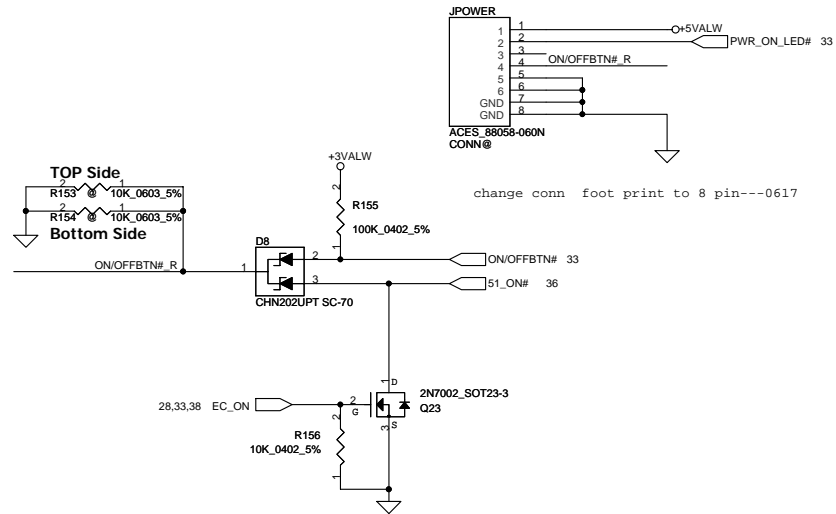


Lid SW

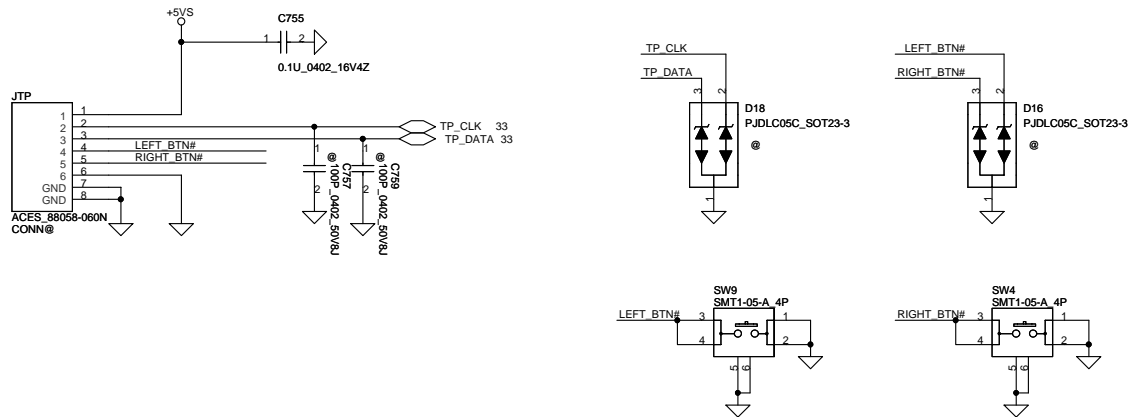


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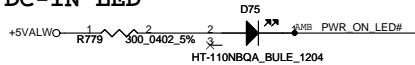
Power Button/ PWR/B



Touch/B Connector



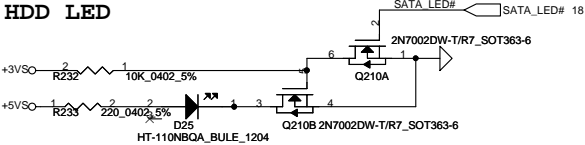
DC-IN LED



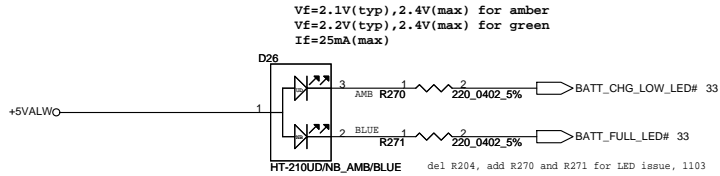
WL&BT LED



HDD LED



BATT CHARGE/FULL LED

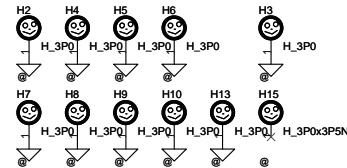


CAP LOCK LED



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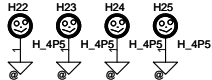
Screw Hole



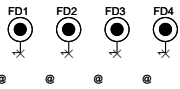
JWLAN



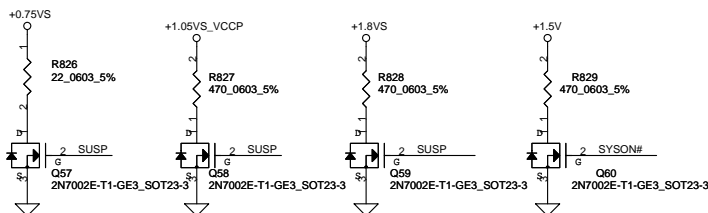
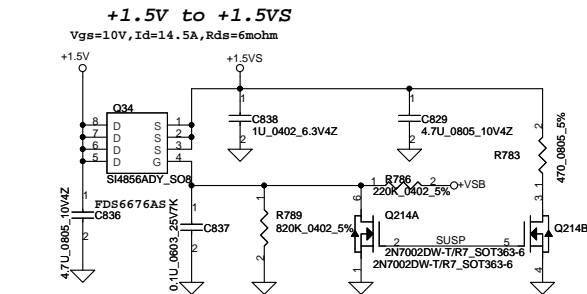
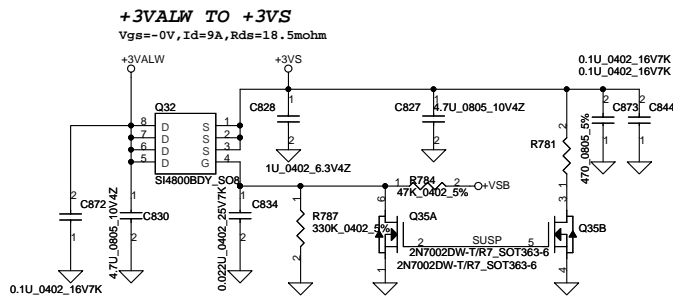
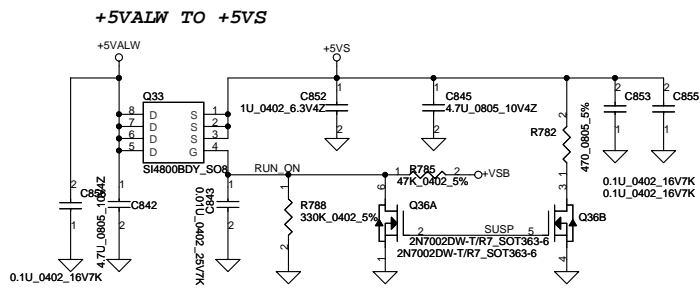
CPU



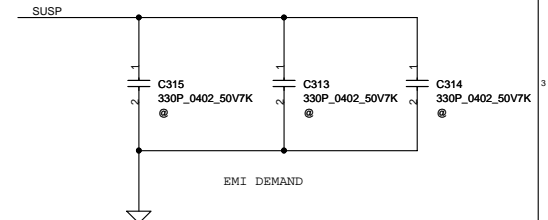
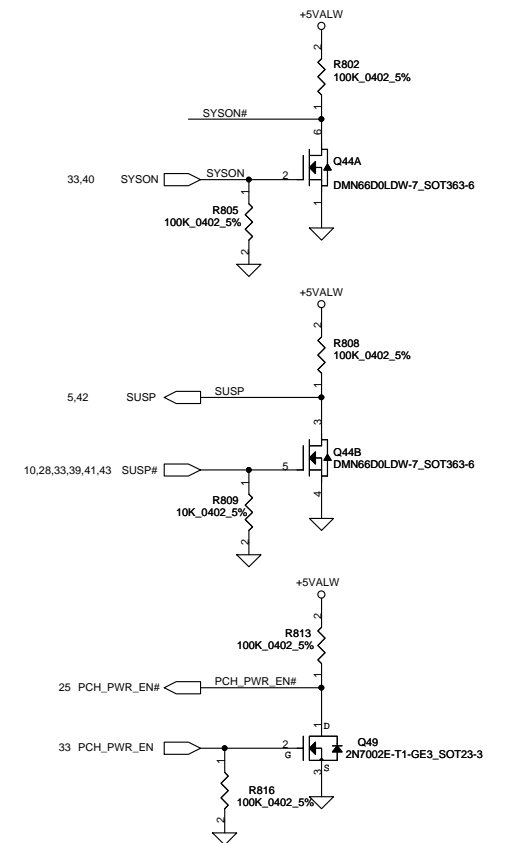
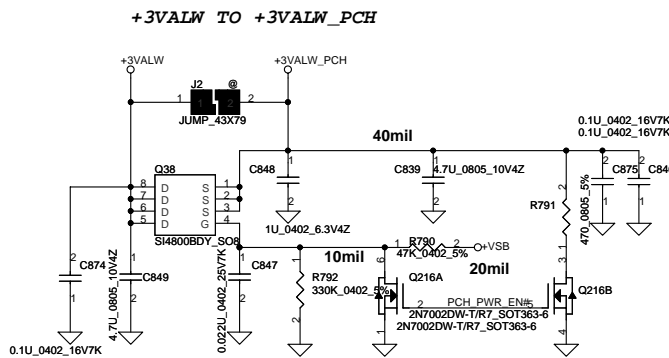
PCB Fedical Mark PAD



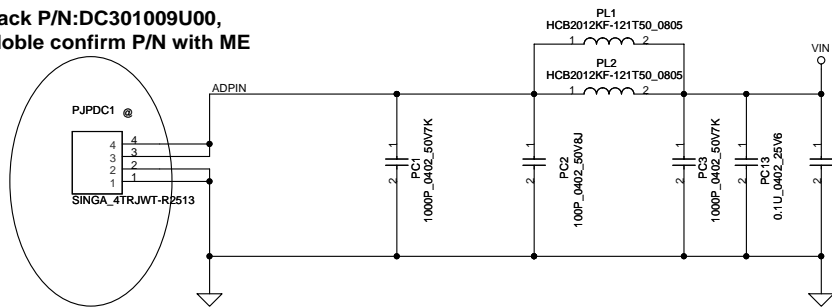
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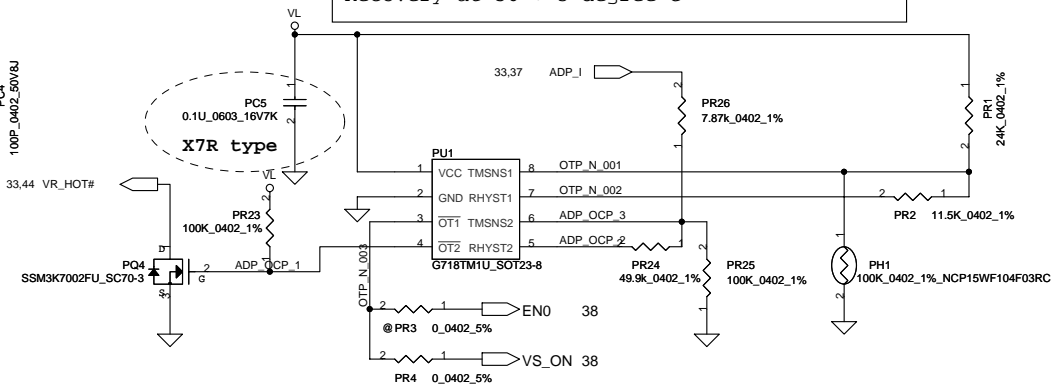
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge



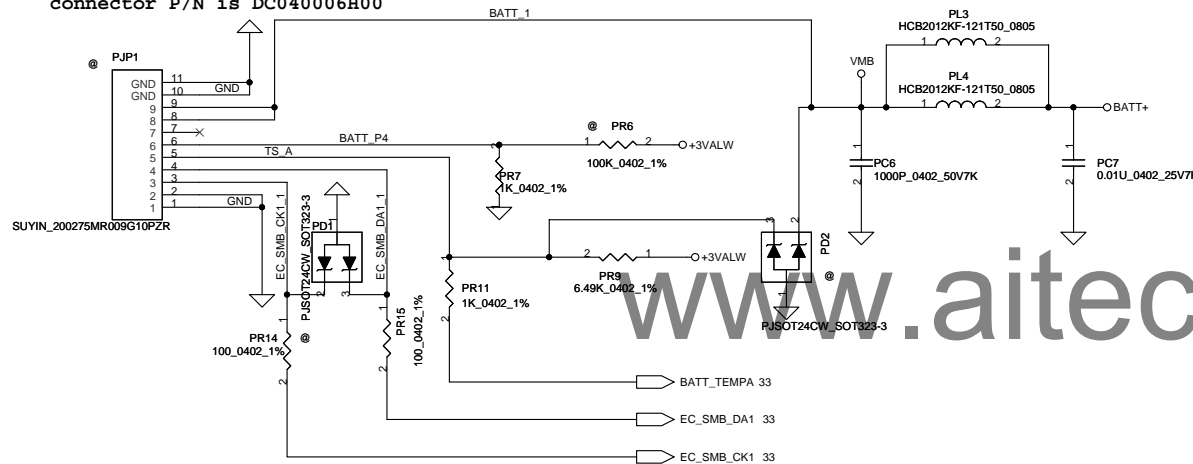
DCIN jack P/N:DC301009U00,
need dogle confirm P/N with ME



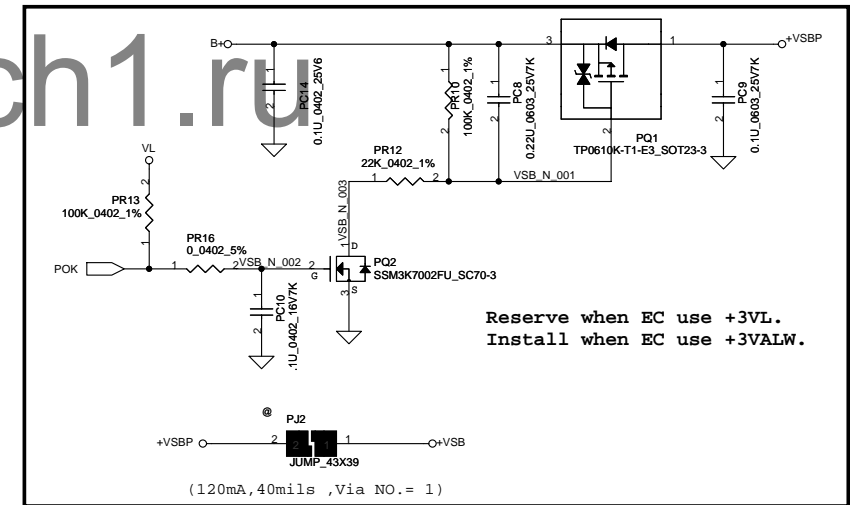
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



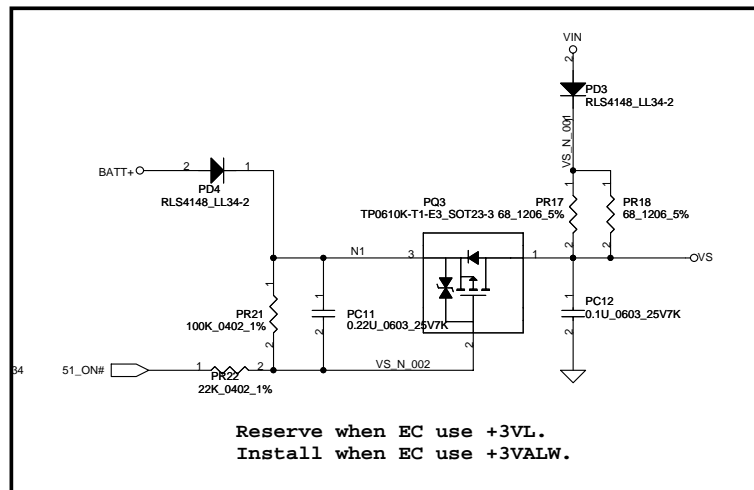
need confirm: ME give us battery
connector P/N is DC040006H00



If EC use 3VL and can not detect VGATE,
must connect EN0

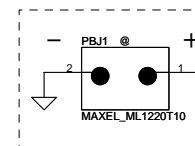


Reserve when EC use +3VL.
Install when EC use +3VALW.



Reserve when EC use +3VL.
Install when EC use +3VALW.

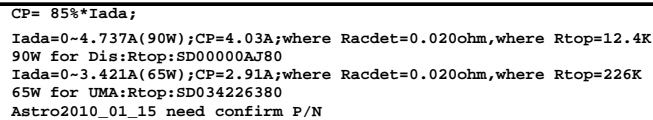
RTC Battery



SP093MX0000

Must close PBJ1

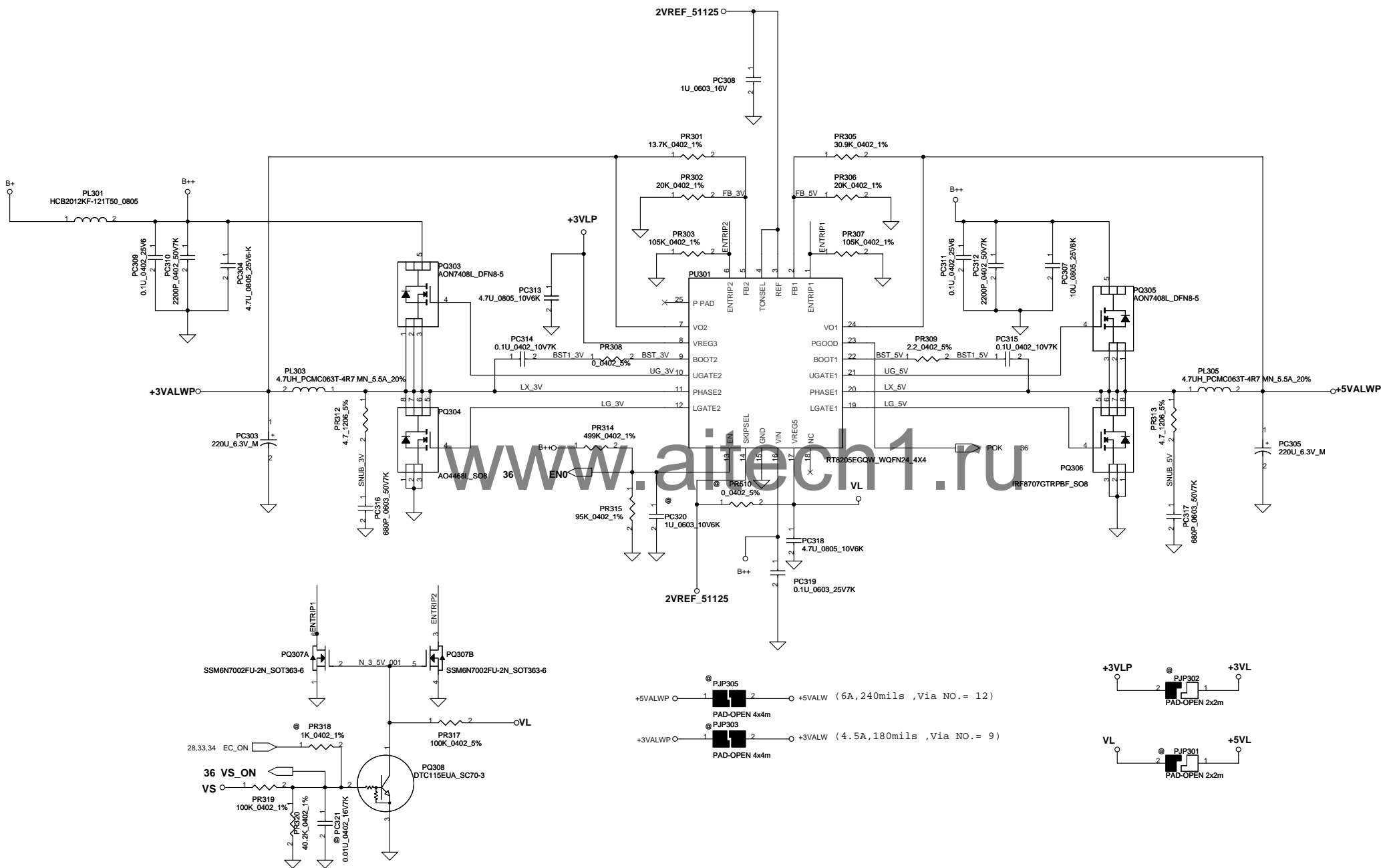
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```
CP model
Vaclim=VREF*(Rbot//Rinternal*(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A
```

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V

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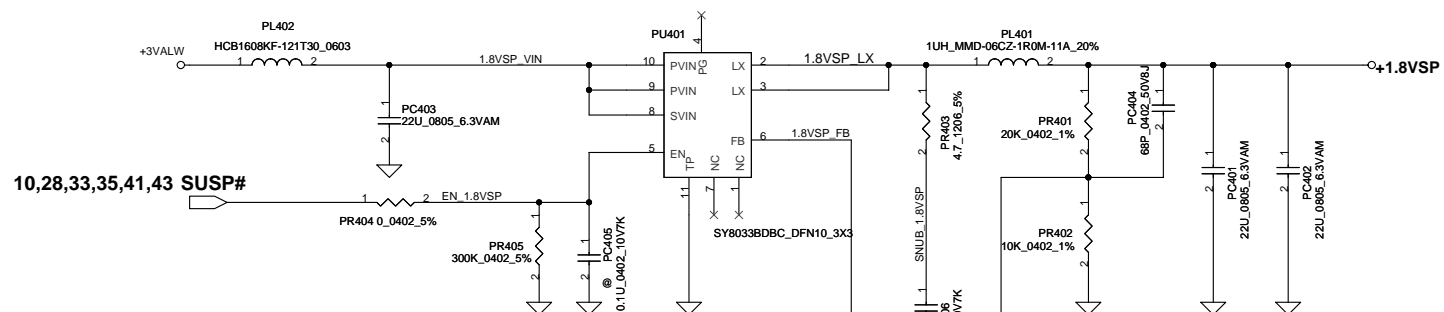
EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

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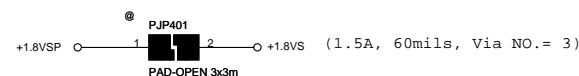
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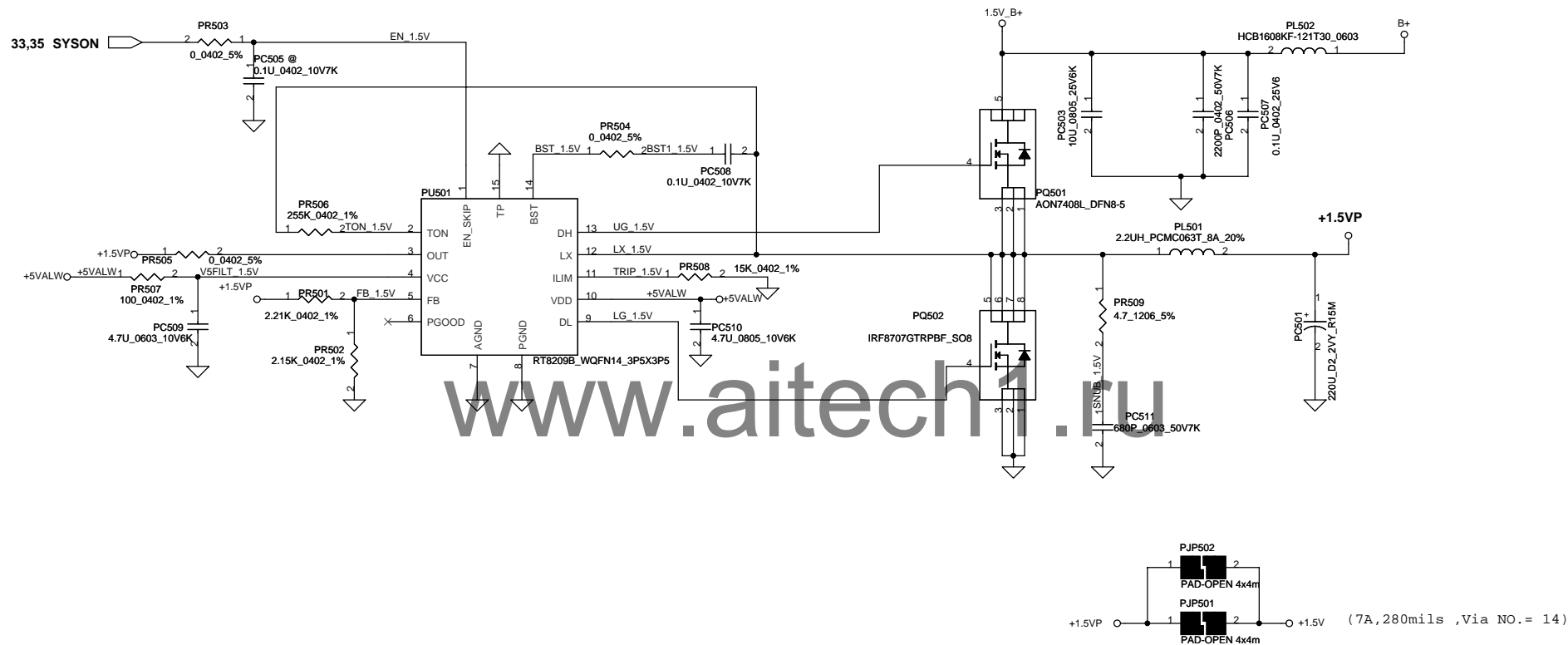
$$<V_o=1.8V> \quad V_{FB}=0.6V$$

$$V_o=V_{FB} * (1+PR401/PR402)=0.6 * (1+20K/10K)=1.8V$$

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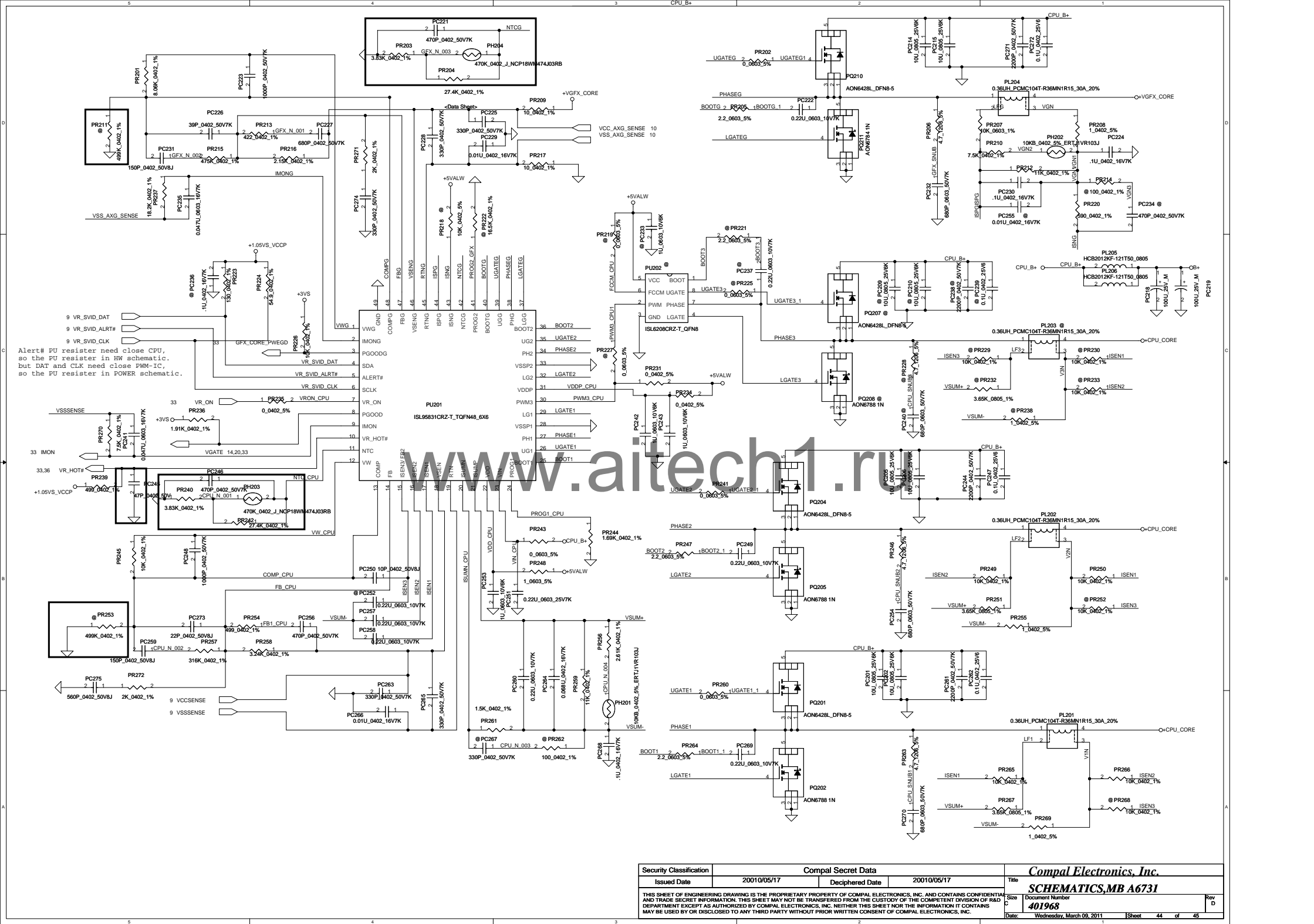


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PIR (Product Improve Record)

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/13	25	Reserve R433	Reserve +3VLW power for VCCPDSW
2	08/13	31	DEL RA17, RA19-->RA19@, change RA16 to 39.2K	Audio MIC sense from B to A
3	08/13	17	Add R432,unpop R572,R1530,U47,C869 for HDMI HPD	HDMI HPD design change
4	08/23	31	change CA9 CA10 to 4.7u(0603)	Audio test Issue
6	08/23	28	Change U142A compare circuit Change U142B compare circuit Change new Bus switch for 3V system Change KB930 programming strap pin	change degug schematic to follow PBL21
7	08/23	34	change LED(D74,D75,D25,D26) to follow ID and ME define	EMI demand
8	09/03	35	Change ODD_EN# from GPIO24 to GPIO68 GPIO24 PU +3VS 10K	GPIO Common design
9	09/03	41	Reserve C729,C730,C731,C732 to +3VS	EMI demand
10	09/03		Reserve C330,C311 on H_PWRGD	EMI demand
11	09/03		Reserve C314,C315,C315 on SUSP	EMI demand
12	09/03		Reserve C850,C851, C854 on SVS	EMI demand

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	09/28	31	change MIC1 from onboard MIC to Conn	change onboard MIC
2	10/22	18	swap HP_R and HP_L	error
3	10/28	20	Del R734, Add R1192 for SUSCLK PD	EC Request, Common Design
4	10/28	10	R114,R115 change to 1K fro SM_VREF	Follow Intel DG
5	10/28	8	R92,R93 change to mount for RSVD6,7	Follow Intel DG
6	10/28	18	Del T72, Add R193 for PCH_GPIO19,Del R182	Follow Intel DG
7	10/28	22	change R314 to 1K for NV_CLE	Follow Intel DG
8	10/28	24	change VCC_SPI to +3VS	Common DG
9	10/28	18	add R438(1M) for HAD_SNC_R PD	Follow Intel DG
10	10/28	5	add C234,C235,C236,C238,C243 for EMI demand	EMI demand
11	10/29	33	add R744,R1211	EC GPIO Common design for USB30_OC# and P_USB#

Revision Change: 0.3 to 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/06	34	Charge LED:del R204, add R270,R271	to fit the SPEC
2	12/06	10	change C137 from 470U to 330U for PWR demand	CPU_CORE CAP COST
3	12/06	20	add C316 for EC demand	EC Request, Common Design
4	12/06	05	XDP:del XDP for ESD demand	ESD DEMAND
5	12/06	31	MIC:add DA10 A-GND	EMI DEMAND
6	12/06	23	PCH_GPIO24:add R439 for 3VALW_PCH PU(reserve)	Follow Intel DG

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